[redacted]

This course explains the implementation of these PCIe gen2 switches

Objectives

- This course describes the hardware implementation of the switch.
- It explains the possible configuration of switch s port: transparent PCI-to-PCI bridge, Non Transparent endpoints and integrated DMA endpoints.
- Partitioning is clarified through use cases.
- Software configuration is detailed.
- Error management and switch event report is also studied.

- Note that AC6 has a long experience of teaching to companies developing avionics systems.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of PCIe gen1 or gen2 is mandatory, see our related courses.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

SWITCH ARCHITECTURE

- Stack, TLP routing, possible port splitting

- Switch core
- DMA modules

RESET AND INITIALIZATION

- Switch fundamental reset sequence
- Boot configuration vector
- SWMODE[3:0] configuration pins
- Enumeration software
- Runtime reconfiguration

LINK AND PHY OPERATION

- Lane reversal
- Link width negotiation in case of bad lanes
- Dynamic link width reconfiguration
- Link speed negotiation
- Link retraining
- Crosslink

HARDWARE IMPLEMENTATION

- Clocking, global reference clock and port reference clock
- Port global clocked mode, port local clocked mode
- Support of spread spectrum clocking

PARTITIONABLE PCI EXPRESS SWITCH

- Associating ports to form a completely independent PCIe switch
- Port configuration, transparent bridge, Non-Transparent (NT) bridge, DMA endpoint
- Multi-function ports
- Port operating mode change
- Highlighting ports supporting DMA function and port supporting NT function
- NT interconnect
- NT mapping table, address translation

DMA OPERATION

- DMA controller registers, remapping them in MEM space
- Descriptor format, list of descriptors
- Multicast support
- Halting or suspending a transfer

SWITCH CORE ARCHITECTURE

- Single VC
- Ingress buffers
- Egress buffers, head-of-line blocking
- Packet routing classes, inter- and intra-partition transfers
- Port arbitration
- Cut-through operation
- Request metering

SWITCH EVENTS

- Signaling an event occurred in one partition to the host processor of other partitions
- Internal error logic, emulating errors, integrated ECC protection
- Reporting errors using AER

MULTICAST

- PCIe multicast specification
- Address type header field
- Transparent multicasting, multicast BAR
- NT multicasting, address and requester ID overlay feature

CONFIGURATION SPACES

- Register organization, global address space
- Indirect access from any function configuration space
- Transparent PCI-to-PCI bridge proprietary registers
- NT endpoint registers
- Switch control and status registers

Renseignements pratiques

Inquiry : 2 days