H6 - Lattice - PCIe 1.1 x1, x4 IP core

This course describes the implementation of the Lattice PCIe core present in ECP2M, ECP3 and SCM FPGA families

Objectives

- Clarifying the architecture of the PCIe core, distinguishing soft IPs from hard IPs (e.g. the Serdes) .
- Developing software to drive the core and achieve desired functionality.
- Highlighting the management of transmit credits through examples.
- Understanding the various parameters that have to be defined in IPexpress GUI.

- This course is delivered by Ac6 engineers, expert on PCIe, who has also developed trainings on PCIe core for Xilinx.

Lattice software (ispLEVER) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of PCI Express 1.1 is recommended, see our course reference I3.
- Experience with Lattice ispLEVER IDE is recommended, see our course reference H2.

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

DAY 1

INTRODUCTION TO LATTICE PCIe CORE

- Core versions.
- Core requirements, data bus width, performance, resource utilization.
- Indicating how each PCIe protocol layer is implemented and what has to be done in the user logic.
- Interfaces.

CLOCK AND RESET INTERFACE

- 125-MHz and 250-MHz clock domains.
- LatticeECP3 and LatticeECP2M PCIe clocking scheme.
- LatticeSCM PCIe clocking scheme.
- PCIe power-up.

TRANSMIT AND RECEIVE TLP INTERFACE

- Understanding the ports of the transmit interface.
- Nullifying a TLP being transmitted.
- Checking transmit credits prior to send Non-Posted, Posted or Completion packets.
- Completion read boundary definition.
- Understanding the ports of the receive interface.
- Transaction layer error detection and management, generating error messages.
- Updating transmit credits for the peer device.
- Address decode logic in the receiver, BAR registers.
- Completion time-out detection.
- ECRC checking and generation.
- Providing the header of a mal-formed packet detected by the user logic.

PHYSICAL LAYER INTERFACE

- Describing all states and transitions of the PCIe LTSSM.
- Signal description.
- Tracking the state of the LTSSM.
- Forcing the transition to specified states, in order to accelerate simulations.
- Multi-lane operation.
- Adapter card concerns.
- MultiChannel Adapter (MCA), LatticeSCM reference design.

DAY2

LINK LAYER INTERFACE

- Describing the APSSM state machine used to control the power states of the link and of the function.
- Getting the state of the link layer.
- Transmitting power messages.
- Receiving power messages.

CONFIGURATION REGISTERS

- Ports used to export the configuration value set by the host firmware.
- Ports used to force the contents of some registers.

- Detailing all registers, type 0 header, PCIe-related registers, power-management related registers, MSI relared registers, advanced error reporting related registers, and serial number register.
- Getting the device ID, necessary to respond to configuration requests.

INTERRUPT AND MSI

- Explaining the disadvantages of legacy interrupts.
- Generating an interrupt assert / deassert message.
- Determining whether the host software supports MSIs.
- Selecting an MSI number and generating the MSI.
- Behavior of the back end logic when the host software allocates less MSIs than requested.

WISHBONE INTERFACE

- Transfer protocol basics.
- Accessing the registers of the configuration space.
- Wishbone interface memory map.
- Description of IP control and status registers.

IP CORE IMPLEMENTATION

- Lattice SCM MACO blocks.
- Creating the IP through IPexpress GUI, explaining each parameter that has to be defined by the user.
- Implementing loopback.
- Total EBR count based on Max TLP size.
- Created files and directories.
- Simulation strategies.
- LatticeECP3 and LatticeECP2M PIPE Simulation.
- Locating the IP.
- Setting Design Constraints.

SCATTER-GATHER DMA CONTROLLER IP CORE

- Device support for SGDMAC core v2.1.
- Scatter-gather DMA principle.
- Arbitration between channels.
- DMA engine.
- System configurations, utilization in a PCIe design to fill / empty transmit / receive FIFOs.

Renseignements pratiques

Durée : 2 jours
Prix : 1350 € HT