[redacted]

## This course covers PowerQUICC devices, such as MPC885

## Objectives

- The course details PowerPC core low level programming.
- It clarifies the operation of bus controller state machines GPCM and UPMs, including SDRAM interface.
- Time Division Multiplexed frame processing is explained.
- A generic interrupt handler supporting nesting is provided.
- The Ethernet controller is described in detail, particularly the auto-negotiation sequence.
- Debug capabilities and real time trace requirements are studied.

*A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as FEC and SCC.*

- *They have been developed with Diab Data compiler and are executed under Lauterbach debugger.*

*A more detailed course description is available on request at training@ac6-training.com*

## *Prerequisites and related courses*

- Experience of a 32-bit processor or DSP is mandatory.
- The following courses could be of interest:
  - Ethernet and switching, reference cours N1 - Ethernet and switching
  - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0

## *Environnement du cours*

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

## *Audience visée*

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

## *Modalités d'évaluation*

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

# Plan

## INTRODUCTION TO MPC8XX

- MPC8XX block diagram : the PowerPC core, the SIU and the CPM modules
- The 3 registers families : GPRs, SPRs, and memory-mapped
- The 860 derivatives features : 85X, 86X, 87X and 88X
- Performance estimation

## PowerPC CORE ARCHITECTURE

- RCPU pipeline, history buffer, isync instruction
- Execution units
- Cache basics
- Load/store architecture
- Sync and eieio instructions

## PowerPC CORE PROGRAMMING

- User registers
- Branch instructions
- Integer load / store instructions
- Integer arithmetic
- The EABI
- Code and data sections
- Cache related instruction
- Exception management at core level : handler table, priority
- MMU basics
- Tablewalk through the descriptor tables description
- TLB entry software loading

## THE SYSTEM INTERFACE UNIT

- The interrupt controller
- MPC8XX hardware configuration at reset : sampling of the configuration word
- Clock synthesizer

## THE EXTERNAL BUS INTERFACE

- Dynamic bus sizing, connection of 8 and 16-bit peripherals
- Single data read and write timing diagrams
- Burst read and write timing diagrams
- Shared resource control
- Bus error, retry

## THE MEMORY CONTROLLER

- Address decoding through BR/OR registers
- GPCM timing parameters explanation
- SDRAM basics
- Connection of an SDRAM, UPM initialization

## CPM BASICS

- Synchronization between RCPU and CP through the Command Register
- DPRAM organization
- The CPM Interrupt Controller
- CPM general purpose timers

- IDMA channels
- General purpose IO : pin configuration

## THE SERIAL INTERFACE

- ISDN basics
- NMSI vs TDM
- SIRAM initialization to support ISDN frames
- Transmit and Receive clock selection from the bank of clocks
- Buffer Descriptor rings allocation
- Buffer chaining
- Transmit and receive interrupts

## THE SERIAL MANAGEMENT CONTROLLERS

- Supported protocols : transparent, UART and auxiliary ISDN channel
- SMC in UART mode
- SMC restrictions compared to SCC
- Initialization sequence : registers, Parameter RAM, Buffer Descriptors

## THE SERIAL COMMUNICATION CONTROLLERS

- The DPLLs : clock recovery
- UART on SCC
- HDLC on SCC
- Ethernet on SCC : 7-wire interface with the transceiver
- Hash table restrictions
- External CAM connection

## THE SPI CONTROLLER

- SPI protocol
- Clock polarity and phase selection
- Transmit and receive sequences

## THE I2C CONTROLLER

- I2C basics
- Upload of SDRAM parameters located in a DIMM serial EEPROM
- Read and Write sequences

## THE USB CONTROLLER

- USB protocol basics
- MPC885 USB controller features
- Hardware interface
- Architecture
- Programming model
- Read and Write sequences
- Initialization sequence

## THE FAST ETHERNET CONTROLLER

- CPM independence
- MII pinout
- 7-wire vs MII transceiver connection
- Buffer descriptor description
- Initialization sequence

## THE MULTI CHANNEL CONTROLLER

- Logic channel vs time slot
- The time slot assignment tables
- Logic channel processing
- Interrupt queues
- Parameterizing the interface to the framer

## THE SECURITY ENGINE

- Encryption basics
- SEC features
- Memory mapping and programming interface
- Crypto channel management
- Master/Slave interface module description
- Initialization sequence

## THE DEBUG PORT

- BDM features : watchpoints and breakpoint
- Programming interface
- BDM restrictions
- Real time trace solution

## Renseignements pratiques

**Renseignements : 5 jours**