This course covers PowerQUICC III MPC854X devices, including MPC8548E

Objectives

- The course details the internal data path, particularly the Ocean crossbar operation.
- Cache coherency protocol is introduced in increasing depth and the benefit of data stashing is explained.
- The e500 core is viewed in detail, especially the SPU that enables Floating point and vector processing.
- The boot sequence and clocking are explained.
- The course details the hardware implementation of the MPC854X.
- A long introduction to DDR1/2 SDRAM operation is done before studying the DDR SDRAM controller.
- An in-depth description of the RapidIO port and the PCI-X port is done.
- The PCI Express bridge implemented in the MPC8548E is also described.
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers, particularly the TCP/IP hardware assistance engine.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
  - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
  - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
  - for any information contact training@ac6-training.com

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as GigaEthernet.
• They have been developed with Diab Data compiler and are executed with Trace32 Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- Experience of a 32 bit processor or DSP is mandatory.
- The knowledge of the following interconnect standards may be required:
  - RapidIO see our course reference cours IC5 - RapidIO 3.0
  - PCI-X, see our course reference cours IC3 - PCI-X 2.0
  - Gigabit Ethernet, see our course reference cours N1 - Ethernet and switching

Environnement du cours

- Cours théorique
  - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
  - Cours dispensé via le système de visioconférence Teams (si à distance)
  - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
  - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

INTRODUCTION TO MPC854X

Overview

- Address map, ATMU, OCEAN configuration
- Local vs external address spaces, inbound and outbound address decoding
- Accessing memory-mapped registers from external master

THE e500 CORE

THE INSTRUCTION PIPELINE

- Dual-issue superscalar control, out-of-order execution, 12-entry instruction queue, 14-entry completion queue
- Execution units: 2 simple Integer Units + 1 Complex Integer Unit
- Dynamic branch prediction using a 128-set 4-way set associative Branch Target Buffer
- Execution timing, rename register operation, instruction serialization, instruction scheduling guidelines

DATA AND INSTRUCTION PATHS

- The Core Complex Bus
- Load store unit
- The LMQ, the store queue, the castout queue
- Store miss merging and store gathering

THE MEMORY MANAGEMENT UNITS

- Thread vs process
- The first level MMU and the second level MMU, consistency between L1 and L2 TLBs
- TLB software reload, page attributes WIMGE
- Process protection, variable number of PID registers and sharing
- MMU implementation in real-time sensitive applications

CACHES

- The L1 caches, PLRU replacement algorithm, 8-way set associativity, cache block and unlock APU
- Cache coherency
- Level 2 cache, partition into L2 cache plus SRAM
- Allocation of data transferred by external masters into the cache : stashing
- e500 coherency module

PROGRAMMING

- Differences between the new Book E architecture and the classic PowerPC architecture
- Floating Point units, Double-Precision FP of MPC8548E
- Signal Processing APU (SPU)
- PowerPC EABI

EXCEPTIONS

- Book E exception handling
- Critical versus non critical
- Handler table
- Syndrome registers, exception nesting, recoverability from interrupt, soft stop
- Core timers

DEBUGGING

- Performance monitoring, counting of events
- JTAG debug
- Watchpoint logic

PLATFORM OPERATION

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- RapidIO transmit clock source selection
- Power-on reset sequence, using the I2C interface to access serial ROM
- Power-on reset configuration
- Boot page translation

DDR SDRAM MEMORY CONTROLLER

- DDR2 operation
- Jedec specification basics
- Hardware interface
- Bank activation, read, write and precharge timing diagrams, page mode
- ECC error correction
- Introduction to the DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

LOCAL BUS CONTROLLER

- Multiplexed 32-bit address and data transfers
- Burst support
- Dynamic bus sizing
- GPCM, UPMs and SDR SDRAM states machines

RapidIO INTERFACE

- Message Unit, direct vs chaining mode operation
- RapidIO doorbell and port-write unit
- Accessing configuration registers via RapidIO packets
- Programming inbound and outbound ATMUs
- Error handling

PCI EXPRESS INTERFACE

- MPC8548E 8-lane PCI Express interface
- Modes of operation, Root Complex / Endpoint
- Programming inbound and outbound ATMUs
- Configuration, initialization

PCI/PCI-X FUNCTIONAL UNITS

- Bridge features
- Read prefetch and write posting FIFOs
- Inbound transactions handling, Outbound transactions handling in both modes
- Support of multiple split transactions in PCI-X mode
- PCI-to-memory and memory-to-PCI streaming

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency

PERFORMANCE MONITOR AND DEBUG FEATURES

- Event counting
- Chaining, triggering
- Watchpoint facility
- Trace buffer

INTEGRATED PERIPHERALS

THE ETHERNET CONTROLLERS

- Frame format with and without VLAN option
- Address recognition, pattern matching
- Buffer descriptors management
- The three-speed Ethernet controllers (TSECs)
- Physical interfaces : GMII, MII, TBI or RGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast
- MPC8548E management of VLAN tags and priority, VLAN insertion and deletion
- MPC8548E quality of service, filer
- MPC8548E FIFO mode

SECURITY ENGINE

- Overview of the encryption mechanism
- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- Link tables

LOW SPEED PERIPHERALS

- Programmable Interrupt Controller
- Interrupt nesting
- Description of the 4 timers / counters
- Message interrupts
- Description of the NS16450/16550 compliant Uarts
- I2C protocol fundamentals

- Transmit and receive sequence

COMMUNICATION PROCESSOR MODULE (On request)

INTRODUCTION TO CPM

- CP operation : peripheral prioritization
- Command register
- DPRAM organization
- IDMA vs SDMA

THE SERIAL INTERFACE

- NMSI versus TDM
- Supported protocols and max data rate
- Transmit and receive clock selection
- Communication initialization sequence
- Buffer descriptor ring allocation in DPRAM
- Buffer chaining

THE MULTI CHANNEL CONTROLLERS

- DPRAM organization
- Time slot vs logic channel
- HDLC channel parameters
- Interrupt queues

THE SERIAL COMMUNICATION CONTROLLERS

- Data encoding /decoding selection
- UART on SCC
- HDLC on SCC
- Ethernet on SCC

FAST ETHERNET CONTROLLER

- 802.3u basics
- MII interface
- Hash tables utility
- Parameter RAM description

ATM BASICS

- UNI and NNI network interfaces
- Cell format
- Virtual connection
- Layer model
- AAL1 layer
- AAL3/4
- AAL5
- Connection establishment

ATM TRAFFIC MANAGEMENT

- The 5 service classes defined by the ATM forum : CBR, VBRrt, VBRnrt, UBR, ABR
- The QoS ATM attributes : PCR/CDVT, CLR, CTD/CDV
- Traffic policy
- Traffic shaping

THE ATM CONTROLLER

- Utopia 2 hardware interface : multi-PHY control
- APC unit
- VCI/VPI of incoming cells lookup
- OAM AAL0 cells management
- ATM/TDM interworking
- ATM controller parameter RAM description
- RxBD and TxBD format according to the adaptation layer

Renseignements pratiques

Renseignements : 5 jours