This course tackles multicore implementation issues

Objectives

- This course describes the multiple types of multicore implementations : SMP, AMP.
- It details the hardware resources required to support SMP.
- Debug issues are also studied.

- ACSYS offers a large set of multicore processor trainings: ARM Cortex-A9MP (reference R6), NXP MPC8641D (reference FC5) and MPC8572E (reference FN10).

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of high-end processor cores is recommended.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

MULTIPROCESSING TYPES

- AMP
- SMP
- BMP

- Applications examples (MPC8641D, MPC8572, Virtex-4, Virtex 5)

HARDWARE REQUIREMENTS

- Exclusive resource management
- MMU page descriptor table, PowerPC tlbsync instruction
- Multi-core interrupt controller
- Inter-Processor Interrupts
- Message passing

MULTITASK IN MULTI-CORE SYSTEMS

- System booting
- Defining shared resources and non-shared resources
- Assigning a number to each core
- Dispatching tasks to a particular core, static approach, dynamic approach
- I/O management, consequence on driver design

CACHE COHERENCY

- Software coherency (Power instructions dcbz, dcbf, dcbi, icbi)
- Hardware coherency : snooping
- Distinguishing two types of cache enabled area : random access vs sequential access, NUMA model

IMPLEMENTING A MULTI-CORE SYSTEM IN A XILINX VIRTEX-4 FX / VIRTEX-5 FXT FPGA

- PLB basics
- Exclusive resource management, lwarx/stwcx.
- Implementing a multi-core interrupt controller
- Synchronizing time bases
- Is SMP possible in a multi-405 FPGA ?

Renseignements pratiques

Inquiry : 2 days