FPGA

Why design with FPGAs & VHDL?

FPGAs are reconfigurable chips for custom digital hardware; VHDL is the language that describes that hardware at the register-transfer level. Together they deliver high performance and low latency for control, vision, networking, and signal processing—without the cost and lead time of an ASIC.

Modern ecosystems accelerate development: AMD/Xilinx **Vivado/Vitis**(with IP Integrator and **Zynq UltraScale+™ MPSoC**) and Intel **Quartus Prime** (with **Platform Designer/Qsys** and **Nios II/V**). Standard interconnects (**AXI**, **Avalon**), **DDR/LPDDR** controllers, **DMA** and **AXI4-Stream** pipelines, high-speed **PCIe**/Ethernet MACs, plus simulation (**Vivado Simulator/ModelSim/Questa**) and on-chip debug (**ILA**/**SignalTap**). Constraints and static timing (**XDC/SDC**) keep designs timing-clean and CDC-safe.

Our **ac6**FPGA & VHDL courses help you master the ecosystem—writing clear VHDL (and optionally Verilog/SystemVerilog), building testbenches, synthesizing and place-and-routing designs, applying timing constraints, and assembling systems with IP blocks, **AXI/Avalon**, and external memory. We also cover embedded processors (MicroBlaze, Nios, Zynq MPSoC), DMA data paths, and practical debug—so your designs are robust, debuggable, and production-ready.

oRV1 RISC-V Architecture This course provides a comprehensive overview of the RISC-V architecture and instruction set for attendees. They will learn the basics of RISC-V, including RISC-V Assembler and Simulator, writing and running assembly code, and RISC-V C Programming. The course covers topics such as interrupt and exception handling, memory management, multiprocessing, and concurrency, performance optimization, hardware and system design, and future developments. Hands-on experience will be provided through lab sessions. 18 h - **Inquiry** oV1 VHDL Language Basics The VHDL Language Basics course is designed to provide professionals with a comprehensive understanding of the VHDL hardware description language. The course covers basic concepts of VHDL, VHDL syntax, combinational logic in VHDL, synchronous logic in VHDL, synthesis and testbenches, and hierarchical conception. These topics are essential for the development of digital circuits and systems using VHDL, and are applicable to a wide range of applications, including the design of FPGA-based systems. The course is suitable for professionals with a basic understanding of digital design concepts and is designed to provide a strong foundation in VHDL language development. 24 h - **Inquiry** oV2 Advanced VHDL for FPGA This training is intended for professional who already knows how to use programmable components but also have to create and test them, it is intended to complement course oV1. 18 h - **Inquiry**