FC5 - MPC8641(D) implementation

This course covers NXP MPC8641 and MPC8641D single- and dual- core Power CPUs

Objectives

- **The course clarifies the architecture of the MPC8641D, particularly the operation of the coherency module that interconnects the e600s to memory and high-speed interfaces.**
- **Cache coherency protocol is introduced in increasing depth.**
- **The e600 core is viewed in detail, especially the Altivec units that enable vector processing.**
- **The boot sequence and the clocking are explained.**
- **The course focuses on the hardware implementation of the MPC8641D.**
- **A long introduction to DDR SDRAM operation is done before studying the DDR SDRAM controller.**
- **An in-depth description of the RapidIO port and the PCI-Express port is done.**
- **The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers.**

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- **Experience of a 32-bit processor or DSP is mandatory.**
- **Knowledge of the RapidIO (see our IC5 - RapidIO 3.0course) and PCI Express bus (see our IC4 - PCI Express 3.0course) is recommended.**

Course Environment

- **Theoretical course**
  - **PDF course material (in English) supplemented by a printed version for face-to-face courses.**
  - **Online courses are dispensed using the Teams video-conferencing system.**
  - **The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.**
- **At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed**

Target Audience

- **Any embedded systems engineer or technician with the above prerequisites.**

Evaluation modalities

- **The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.**
- **Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented**
- **At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.**
  - **In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.**

Plan

MPC8641D OVERVIEW

Overview

- e600 core, usage of a dual core device
- Coherency Module
- Examples of data flow through the MPC8641D
- Address map, local access windows
- Outbound and inbound address translation windows

e600 CORE

PIPELINE

- Pipeline basics
- Introduction to e600 pipeline
- e600 pipeline implementation
- Execution serialization, purpose of the isync instruction
- Branch management
- Guarded memory
- Coding guidelines
- Performance monitor

INTERNAL DATA AND INSTRUCTION PATHS

- L1 and L2 cache loading, hit under miss
- The MSS [Memory Sub System]
- The load fold queue
- The store miss merging advantage when several vectors must be stored
- The BIU [Bus Interface Unit]
- Purpose of sync and eieio instructions

L1 AND L2 CACHES

- Cache basics
- e600 L1 cache : PLRU algorithm, HID0/ICTRL programming interface, way locking
- L1 data cache flush
- Transient load instructions benefits
- L2 cache organization
- L2 replacement algorithm selection, L2 locking
- Cache coherency basics
- MESI snooping sequences involving 2 e600s and a PCI Express master

e600 PROGRAMMING

- User and supervisor registers
- The system call communication path between applications and RTOS
- Integer load / store instructions, boolean semaphore management
- IEEE754 basics
- FPU operation : FPSCR register, IEEE vs non-IEEE mode
- The EABI
- Code and data sections, small data areas benefits

ALTIVEC

- **Altivec introduction, SIMD processing**
- **Intra vs inter element instructions**
- **Altivec registers, VSCR initialization**
- **ANSI C extension to support vector operators, new C types, new castings, vector declaration and initialization**
- **Altivec implementation on the e600 : the VALU and the VPU execution units**
- **Data streams management**
- **EABI extension to support Altivec**

THE MEMORY MANAGEMENT UNIT

- **MMU goals**
- **Enabling 4 additional BATs**
- **32-bit or 36-bit real address size selection**
- **WIMG attributes definition, page and block access rights definition**
- **Page protection through VSID selection**
- **TLB organization, TLB software management**
- **Page translation : PTEG selection, tablesearch, PTE content**
- **Software vs hardware TLB reload**
- **MMU implementation in real-time sensitive applications**

THE EXCEPTION MECHANISM

- **Exception state saving and restoring through SRR0/SRR1 registers**
- **Exception management**
- **Recoverable vs non recoverable interrupts**
- **Requirements to support exception nesting**
- **Performance monitor**

MPC8641D INFRASTRUCTURE

RESET AND CLOCKING

- **Platform clock**
- **RapidIO transmit clock source selection**
- **Power-on reset sequence, use of the I2C interface to access a serial ROM**
- **Power-on reset configuration**
- **Boot page translation**

MPX COHERENCY MODULE

- **I/O arbiter**
- **MPX arbiter**
- **Transaction queue**
- **Global data multiplexor**
- **MPX interface**

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- **Open PIC architecture compatibility**
- **Interrupt nesting**
- **Description of the 4 timers / counters**
- **Message interrupts**
- **e600-to-e600 interrupt capability**

DDR-SDRAM MEMORY CONTROLLER

- **DDR2 operation**
- **Command truth table**
- **Hardware interface**
- **Refresh types**
- **Bank activation, read, write and precharge timing diagrams, page mode**
- **ECC error correction**
- **Initial configuration following Power-on-Reset**
- **Address decode**
- **Timing parameters programming**
- **FCRAM interface commands**

LOCAL BUS CONTROLLER

- **Multiplexed 32-bit address and data transfers**
- **Burst support**
- **Dynamic bus sizing**
- **GPCM, UPMs and SDR SDRAM states machines**

INTEGRATED DMA CONTROLLER

- **Priority between the 4 channels**
- **Support for cascading descriptor chains**
- **Scatter / gathering**
- **Selectable hardware enforced coherency**
- **Ability to start DMA from external 3-pin interface**

SERIAL RapidIO INTERFACE

- **Message Unit, direct vs chaining mode operation**
- **RapidIO doorbell and port-write unit**
- **Accessing configuration registers via RapidIO packets**
- **Programming inbound and outbound ATMUs**
- **Error handling**

PCI EXPRESS INTERFACE

- **Modes of operation, Root Complex / Endpoint**
- **Byte swapping**
- **Transaction ordering rules**
- **Programming inbound and outbound ATMUs**
- **Configuration, initialization**

PERFORMANCE MONITOR AND DEBUG FEATURES

- **Event counting**
- **Threshold events**
- **Watchpoint facility**
- **Trace buffer**

MPC8641D INPUT / OUTPUT PERIPHERALS

THE ETHERNET CONTROLLERS

- **802.3 specification fundamentals : the 3 layers PHY, MAC and control**
- **Frame format with and without VLAN option**
- **Address recognition, pattern matching**
- **Buffer descriptors management**
- **The enhanced three-speed Ethernet controllers (eTSECs)**
- **Physical interfaces : GMII, MII, TBI or RGMII**

- **Buffer descriptor management**
- **Layer 2 acceleration accept or reject on address or pattern match**
- **256-entry hash table for unicast and multicast**
- **IPv4, TCP and UDP checksum verification and generation**
- **Quality of service support**

I2C CONTROLLERS

- **I2C protocol fundamentals : addressing, multimaster operation**
- **Transmit and receive sequence**

SERIAL INTERFACE

- **Introduction to UART protocol**
- **Description of the NS16450/16550 compliant Uarts**
- **Flow control signal management**

Renseignements pratiques

Duration : 5 days
Cost : 2100 € HT