FCC3 - e200z7 implementation

This course covers the e200z7 core present in NXP MPC56XX MCUs

Objectives

- This course has 5 main objectives:
  - Learning the exception mechanism, providing guidelines to implement nesting
  - Explaining the operation and initialization of the MMU and caches
  - Highlighting the cache coherency issues and explaining the snooping
  - Detailing low level programming, particularly the floating-point and SPE instructions
  - Describing the debug units.
- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- For any information contact training@ac6-training.com

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32-bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

CORE ARCHITECTURE

- e200 core family
- Main blocks, pipeline, MMU, cache, timers, debug unit

INSTRUCTION PIPELINE

- Prefetch queue
- Decode / dispatch stage
- Concurrent Instruction Issue Capabilities
- In order execution
- Completion, register write-back
- Dynamic vs static branch prediction
- Guarded memory

SUPERVISOR PROGRAMMING, EXCEPTION MECHANISM

- Building the exception vector table
- Exception taking sequence
- Implementing nesting among maskable interrupts
- Reset sequence

INSTRUCTION AND DATA PATH

- Studying cache reload transients
- Line-fill buffers
- Memory synchronization
- Spin-lock routine

MEMORY MANAGEMENT UNIT

- Assigning attributes to pages
- Assigning access permissions to page
- Page protection
- MMU-related exceptions
- 64-entry, fully associative TLB
- TLB software reload, using MAS registers

LEVEL ONE CACHES

- 4 way set-associative Harvard instruction and data caches
- Data and instruction prefetch instructions
- Cache software control, cache line lock
- Coherency issues when cacheable pages are shared with DMA
- Cache parity and EDC protection
- Cache memory access via software

PARALLEL SIGNATURE UNIT

- System integrity checking
- Monitoring the internal CPU read and write buses

USER-LEVEL PROGRAMMING

- EABI, small sections
- Tricky instructions

- C coding guidelines

SIGNAL PROCESSING ENGINE

- Half-precision floating-point format
- Floating point simple precision & double precision scalar instructions
- Floating point vector instructions
- Fixed point vector instructions, fractional format
- Vector data arrangement instructions
- Managing a circular buffer

VARIABLE LENGTH ENCODING

- VLE storage addressing
- MMU extensions
- Summary of instruction set

CORE TIMERS

- 64-bit time base
- Decrementer
- Software watchdog

DEBUG

- Performance monitor
- Nexus Class 3+ real-time development unit
- Hardware instruction and data breakpoints
- Debug interrupt
- Debug notify halt instruction
- Using debug data acquisition message
- Watchpoint programming
- Instruction and data trace

POWER MANAGEMENT

- Power-saving modes: doze, nap, sleep, and wait
- Debug considerations for power management

Renseignements pratiques

Duration : 3 days
Cost : 2290 € HT