This course covers the VPX and Open VPX VITA standards

Objectives

- Providing VMEbus-based systems with support for switched fabrics.
- Describing the new 7-row high speed connector rated up to 6.25 Gbit/s.
- Clarifying alignment and keying requirements.
- Supporting PMC,FMC (VITA 57) and XMC (VITA 42) mezzanines.
- Implementing Hybrid backplanes to accommodate VME64, VXS and VPX boards.
- The course also explains the interoperability improvements offered by the Open VPX standard through the implementation of predefined system topologies.

- This course has been delivered several times to companies developing defense and avionics equipments.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- Basic knowledge of high-speed serial interconnect is recommended, such as PCIe, SRIO or Gigabit/10G Ethernet.
- See our courses on PCI Express reference IC4 - PCI Express 3.0course, RapidIO reference IC5 - RapidIO 3.0course, Gigabit Ethernet, reference N1 - Ethernet and switching course and 10 Gigabit Ethernet, reference N3 - Ethernet 10 Gigabit course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

VPX STANDARD

- Objectives of this standard
  - Limitations of shared bus system
  - Implementation of a switch fabric
  - Evolutionary roadmap for VME users
- Overview, definitions
- System signals
  - Power supply
  - System controller
- Board form factor
  - Connector pin definitions, P0 utility connector
  - Alignment and keying
  - Electrical budgets for protocol standards
  - Power wafer current ratings
  - Connector pin definitions, P1
  - 3U modules, P2 connector, differential vs single-ended pinout
  - 6U modules, P2-P6 connectors
- Backplane
  - Power delivery
  - Backplane fabric connections electrical requirements
  - System management signals connection
  - Hybrid backplane
  - Example: five slot fabric full mesh backplane routing

VME, SRIO, PCI EXPRESS AND ETHERNET ON VPX FABRIC CONNECTOR

- VME bus signals mapping on VPX
  - SYSRESET management
  - P3-P6 connector pin mappings
- Serial RapidIO on VPX fabric connector
  - Assigning Serial RapidIO ports to the VPX P1/J1 connector
- PCI Express on VPX fabric connector
  - Reference clock
  - System reset
  - Assigning PCIe ports to the VPX P1/J1 connector
- Gigabit Ethernet control plane on VPX fabric connector
  - 1000BASE-BX or 1000BASE-KX interface on each of the Ultra-Thin Pipe ports
- Gigabit Ethernet on VPX fabric connector
  - Pipe definition, Ethernet Fat Pipe 10GBASE-KX4, 10GBASE-BX4, Ultra Thin Pipe 1000BASE-KX, 1000BASE-BX

PMC/XMC REAR I/O FABRIC SIGNAL MAPPING ON 3U AND 6U VPX MODULES STANDARD

- Mezzanine card Rear I/O pattern maps
- Mezzanine Type label
- 3U vita 46.0 connector pin mapping
- 6U vita 46.0 connector pin mapping
- Electrical specifications

REAR TRANSITION MODULE

- General arrangement of front and read modules
- Alignment keying sockets
- Current and power per RTM slot
- Connector pin definitions RP0

OPEN VPX

- Bringing versatile system architectural solutions to the VPX market
- Description of a series of standard profiles
- System Interoperability Diagram with interface content
- Profiles definition
- Backplane profile topologies: centralized, distributed, hybrid
- Mechanical requirements
- Slot profile
- Backplane profile
- Module profile
- Standard development chassis profile

Renseignements pratiques

Inquiry : 2 days