IS1 - S-FPDP

This course covers Serial-FPDP (VITA 17)

Objectives

- The course details the hardware implementation of S-FPDP and clarifies the operation of 8b10b encoder/decoder.
- Transfer sequences captured with the Absolut-Analysis equipment are studied to explain the frame formats and the flow control mechanism.
- The course describes the parameterizing of the Xilinx S-FPDP IP based on Multi Gigabit transceiver integrated in Virtex FPGAs.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge on serial buses.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION

- Benefits of S-FPDP with regard to other high-speed interconnects
- Layered protocol
- Allowed bit-rates and distances

- Copper vs optic fiber media
- Point-to-point protocol
- Relationship with FibreChannel
- Introduction to FibreChannel low layers

CONVERTING PARALLEL-FPDP SIGNALING INTO S-FPDP SIGNALING

- Overview of P-FPDP
- Strobe signals
- Frame delimitation
- Flow control
- Data frame types

S-FPDP SYSTEM SPECIFICATIONS

- Basic systems, no feedback channel
- Flow control, related ordered sets, FIFO management
- Taking into account the cable length
- Bi-directional data flow
- Copy mode, multicast emulation, options for re-transmitting the clock
- Copy / loop mode, benefit of a feedback channel to enable flow control
- Error recovery
- Exercice : studying traces captured by the Absolut-Analysis equipment to understand the flow control mechanism

LINK SPECIFICATIONS

- Typical S-FPDP process
- Understanding 8b10b coding scheme
- Runtime DC balance through disparity calculation
- Requirements for clocks
- Avoiding underrun and overrun, using an elastic buffer
- List of ordered sets
- Electrical characteristics
- Fiber frame types
- Exercice : studying traces captured by the Absolut-Analysis equipment

XILINX S-FPFP IP

- MGT block diagram
- Parameterizing the MGT to support S-FPDP
- CoreGen
- Focus on the analog part of the transceiver

Renseignements pratiques

Duration : 2 days
Cost : 1250 € HT