MV2 - MARVELL MV64560 implementation

This course covers Marvell Discovery V devices

Objectives

- The course describes the MV64560 internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the message unit.
- Operation of the PCI Express interface is detailed in Root Complex mode as well as in Endpoint mode.
- A long introduction to DDR SDRAM is done prior to describe the DDR SDRAM controller operation.
- The course focuses on the hardware implementation of the DDR SDRAM.
- The training explains how to implement chained DMA transfers, by using either IDMA channels or XOR engines.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.

- This course has been delivered several times to companies developing defence and avionics systems.

A more detailed course description is available on request at training@ac6-training.com

Pre-requisites

- Knowledge of PowerPC 60X / MPX bus. See our courses on NXP and IBM Microelectronics PowerPCs.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- PCI express, reference IC4 - PCI Express 3.0course
- USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

OVERVIEW

- 5-bus architecture, organization of a board based on MV64560
- Frequency domains, fast path between CPU and SRAM / SDRAM
- Internal crossbar
- Master de-mux programming, address decode windows
- Slave mux programming, pizza arbiters operation
- Compatibility with MV64460

CPU INTERFACE

- CPU address space decoding
- Protection windows
- Arbitration, multi-processor operation
- CPU slave operation
- CPU master operation (60X mode)
- Cache coherency
- Deadlock avoidance

DDR1/2 INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- Differences between DDR1 and DDR2
- DDR2 on-die terminations
- Initialization sequence
- DDR1/2 SDRAM controller
- Page management
- Transaction ordering
- Cache coherency
- ECC and read-modify-write transactions
- Low power modes

DEVICE CONTROLLER

- Functional description
- Address and data multiplexing
- Connecting 8/16 bit devices
- External acknowledgement
- Pack / unpack and burst support
- NAND flash support, boot from NAND flash

PCI INTERFACE

- PCI bus arbitration
- Master operation in PCI and PCI-X mode
- Target operation in PCI and PCI-X mode
- PCI-to-PCI configuration transactions
- Address decoding

PCI-EXPRESS x4 INTERFACE

- Integrated low power SERDES PHY
- x1, x4 link
- Operating as either Root Complex or Endpoint
- Link initialization
- Arbitration and ordering

- Messaging unit

GENERAL PURPOSE INPUT/ OUTPUT PINS

- GPIO port, functional description
- Interrupt request inputs
- Multi Purpose Pin multiplexing

INTERRUPT CONTROLLERS AND TIMERS

- Timers / counters
- Interrupt controller functional description
- Priority mechanism

TWSI CONTROLLER AND RESET

- I2C protocol basics
- TWSI controller functional description
- Master write sequence, master read sequence
- Slave write sequence, slave read sequence
- Reset pins and configuration
- Serial ROM initialization
- Requirement for an external Central Resource CPLD

IDMA CHANNELS

- IDMA address decoding
- Target unit and attributes programming
- Normal mode vs chained mode
- Transfer descriptors, descriptor ownership
- DMA interrupts

XOR ENGINES

- State machine : Active, Inactive and Paused states
- XOR operation mode
- CRC32 operation mode
- DMA operation mode
- Memory Initialization operation mode
- ECC error cleanup operation mode
- XOR Engines interrupts

16550 COMPATIBLE UARTs

- FIFO mode
- Flow control
- Transmit sequence
- Receive sequence

USB2.0 PORTS

- Address decoding
- Integrated PHY
- USB host operation, EHCI specification support
- USB device operation, Endpoint configuration

GIGABIT ETHERNET CONTROLLERS

- Interface to the PHY
- SGMII support
- Dedicated DMA

- Transmit weighted round-robin arbitration
- Backpressure mode
- Transmit and receive sequences
- Management interface
- Synchronous FIFO interface

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT