NS2 - MARVELL 88E6161 Ethernet switches

This course covers Marvell Link Street Gbps Soho switches

Objectives

- Providing the basic knowledge on 802.3 and 802.1.
- Understanding the parameters that determine the QoS.
- Implementing the Dynamic Queue Limit architecture.
- Description of the Address Lookup engine.
- Implementing the Distributed Switch Architecture.
- Becoming familiar with the API defined by Marvell.

- This course has been delivered several times to companies involved in the design of embedded equipments.

Practical labs using the Marvell GUI allow attendees to understand the various operation modes offered by this class of switch devices.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of IEEE 802.3 and IEEE 802.1: see our course Ethernet and switching, reference N1 - Ethernet and switchingcourse
- Knowledge of IEEE 1588 may also be needed: see our N2 - IEEE1588 - Precise Time Protocolcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

100 Mbps ETHERNET BASICS

- MAC layer, frame format, frame filtering
- Full duplex Ethernet vs CSMA/CD
- PHY layer, scrambling, 4b/5b coding, NRZI
- Auto-negotiation, utilization of FLPs
- MII

1 Gbps ETHERNET BASICS

- 1000BASE-T
- 1000BASE-X
- GMII transfer protocol, RGMII, SGMII

802.1Q BASICS

- Spanning tree algorithm, RSTP, MSTP
- VLAN tag, selecting one tree and selecting the priority of a frame
- Port states
- Automatic address learning
- Automatic address aging
- Handling multicasts, GVRP, IGMP snooping

INTRODUCTION TO 88E6161 SWITCHES

- Block diagram, ports 0-3 features
- Port 4 and port 5 operating modes
- Pin strapping
- Application examples

BASIC SWITCH FUNCTIONS

- MACs
- PPU
- RMON registers
- Basic switch operation
- 802.1X source address authentication
- Multiple FIDs in VLAN systems

NORMAL PORTS

- Ingress policy
- VLANs
- Special frame handling
- QOS qualification
- Port-based Ingress Rate Limiting
- Queue Controller
- Egress policy

PROVIDER PORTS

- Distinguishing S-TAG from C-TAG
- Customer-to-Provider trafic
- Provider-to-Customer traffic
- Customer-to-Customer traffic
- Provider-to-Provider traffic

DSA PORTS

- Implementing control traffic between switches and management CPU
- Forward DSA tag
- TO_CPU DSA tag
- FROM_CPU DSA tag
- Interconnecting switches by using cross-chip links
- Switch handling of DSA frames
- Secure Control Technology

ADVANCED SWITCH FUNCTIONS

- Spanning Tree support
- Ingress MGMT/BPDU frame detection
- Proper connection to a management CPU and to a router
- Port mirroring
- Port trunking support
- PTP implementation

ACCESSING SWITCH REGISTERS

- The 16 register groups
- Multi-chip addressing mode
- Single-chip direct access to registers
- Remote Management frames

PHY LAYER

- Transmit PCS and PMA
- Receive PCS and PMA
- Power management
- Far End Fault indication
- Auto MDI/MDIX crossover
- LED interface
- Accessing PHY registers, MDC/MDIO interface
- Auto-configuration

SOFTWARE ARCHITECTURE

- DSDT suite
- Multi-layer architecture
- OS independency
- Source code organization
- Platform specific routines
- SMI interface functions
- Switch driver layer
- API layer
- Interrupts

Renseignements pratiques

Duration : 3 days
Cost : 1650 € HT