P1 - PPC405 core implementation

This course covers the IBM Power 405 core

Objectives

- A boot firmware that initializes the MMU has been developped to explain the boot sequence.
- Internal debug facilities are described.
- OCM memory benefits compared to cache are highlighted.
- The course focusses on 405 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- A DFT has been developed to explain how to use mac instructions.
- The PLB and OCM ports as well as debug related signals are described to facilitate the hardware implementation.

- This course has been delivered several times to engineers developing ASICs based on PPC405 and to engineers implementing Xilinx FPGAs containing PPC405 core(s).

Labs are compiled with Diab Data compiler and run under Lauterbach Trace32 debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO 405

- Architecture of a 405-based System-on-Chip
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped

THE CORE ARCHITECTURE

- 5-stage pipeline operation
- Instructions flows through the pipeline
- Speculative execution, guarded memory, SGR register
- Serialization : prefetch barrier implementation by means of unconditional branch instructions, isync instruction
- Cache basics : organization, replacement algorithm, write policies
- Data flow between external memory and caches
- Cache programming interface
- Memory Management Unit : memory attributes definition (cache enabled / cache inhibited, copyback / writethrough)
- Translation Lookaside Buffer initialisation
- Parity control for caches and UTLB
- Cache control and debugging features
- Load / store buffer, sync instruction

PowerPC ARCHITECTURE FOR EMBEDDED APPLICATIONS

- Branch instructions
- System call instruction
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions
- Arithmetical and logical instructions
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT
- Reset

INTEGRATED DEBUG FACILITIES

- JTAG debug
- Logic analyser connection through Mictor connectors
- The 405 instruction trace port
- Hardware vs software breakpoints

HARDWARE IMPLEMENTATION OF THE PPC405 CORE

- External connections
- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- The OCM busses
- Instruction-side local bus interface
- Data-side local bus interface
- DCR interface

APU CONTROLLER

- Connection to the native instruction pipeline
- External coprocessor module
- Software interface
- Class of instructions
- Developing a custom instruction set relying on an external coprocessor

Renseignements pratiques

Duration : 3 days
Cost : 1650 € HT