P3 - PPC464 core implementation

This course covers the IBM Power 464 core

Objectives

- A boot firmware that initializes the MMU has been developped to explain the boot sequence.
- Internal debug facilities are described.
- The course focuses on PPC464 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- A DFT has been developed to explain how to use MAC instructions.
- The Floating Point Unit operation is described.
- The PLB ports as well as debug related signals are described to facilitate the hardware implementation.

- This course has been delivered several times to engineers developing ASICs based on PPC464.

Labs are compiled with GNU compiler and run under Lauterbach Trace32 debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO PPC464FP-H90

- Internal architecture overview
- Highlighting instruction and data paths
- Clocking
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped
- CoreConnect-based SOCs

THE CORE ARCHITECTURE

- Pipeline basics
- 7-stage pipeline operation
- Speculative execution, guarded memory
- Serialization
- Cache basics
- Cache programming interface
- Process vs thread
- Memory Management Unit
- 36-bit real address space
- Translation Lookaside Buffer initialisation
- Cache control and debugging features
- Load / store buffer, speculative loads, msync and mbar instructions

BOOK E COMPLIANT CORE

- Booke E objectives
- Branch instructions
- Addressing modes
- Load / store instructions
- Semaphore management with lwarx / stwcx. Instructions
- Arithmetical and logical instructions, shift and rotate instructions
- Floating point unit, compliancy with IEEE754
- Processing denormalized FP numbers
- Floating point arithmetic instructions
- FP-to-integer and integer-to-FP casting
- The PowerPC EABI
- Cache related instructions
- 16-bit mac instructions to develop fixed point DSP algorithms
- 2-cycle multiply option
- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating when an exception is taken
- Core timers : PIT, FIT and WDT

INTEGRATED DEBUG FACILITIES

- JTAG emulator use
- The 464 instruction trace port
- Real time trace when the PowerPC core executes cached instructions
- Hardware vs software breakpoints

HARDWARE IMPLEMENTATION OF THE PPC464 CORE

- Signal naming convention
- External connections
- Clock and power management interface

- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side PLB interface
- Data-side PLB interface
- DCR interface

Renseignements pratiques

Duration : 3 days
Cost : 1650 € HT