ac6

M5 - 440GP/GX implementation

This course covers AMCC 440GP and 440GX processors

Objectives

- The course explains how to design a 440GX board.
- DDR SDRAM operation is described in order to understand the parameterizing of the memory controller.
- Book E PowerPC architecture is studied, especially the MMU.
- The course provides examples of internal peripherals software drivers.
- Gigabit Ethernet controller and TCP/IP Acceleration Hardware are viewed in detail.
- The training focusses on data path between PCI-X bus and internal PLB bus.

- This course has been delivered several times to companies developing embedded equipments (multimedia systems and avionics systems).

- A chapter on Linux porting can be appended on request.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI-X bus is recommended, see our course reference IC3 - PCI-X 2.0course.
- Knowledge of Gigabit Ethernet is recommended, see our course reference N1 - Ethernet and switchingcourse.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO 440GP/GX

- Block diagram
- Internal concurrent transfers examples
- Hardware introduction
- 440GP/GX mapping
- Programming model
- Comparison between 440GP and 440GX

CORECONNECT PROGRAMMING INTERFACE

- PLB arbiter, OPB arbiter and PLB-to-OPB bridge configuration
- Bus errors recovering from syndrome registers
- PLB performance monitor

440 CORE

- Pipeline operation
- Internal caches
- CCR0 register
- Speculative loads, storage ordering and synchronization : msync & mbar instructions
- MMU

BOOK E COMPLIANT CORE

- Branch instructions
- Addressing modes, load & store instructions
- Integer instructions
- 16-bit mac instructions
- Exception management
- Core timers
- PowerPC EABI
- JTAG emulator use
- Real time trace

CLOCKS, RESET AND POWER MANAGEMENT

- Clocks synthesizer
- Low power modes
- Reset
- Boot routine example
- IIC bootstrap controller

INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS

- Interrupt masking and acknowledgement e
- Critical interrupt handlers using vectorization

THE INTERNAL SRAM

- Write-through cache, understanding the data and instruction path
- Performance monitor
- SRAM utilization - base address definition
- Access errors

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation
- Jedec specification basics
- Hardware interface
- Bank activation, read, write and precharge timing diagrams
- ECC error correction
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming

THE EXTERNAL BUS CONTROLLER

- External bus pinout, driver enables
- Dynamic bus sizing
- Address decoding
- Timing parameters initialization
- Device-paced transfers
- External bus master interface

THE PCI-X BRIDGE

- Data flows
- Inbound an outbound transactions handling
- Address mappings
- Synchronization between CPUs : the MSI registers
- I2O messaging unit, passing messages between processor nodes
- Boot modes, initialization / Reset sequence

THE 4 DMA CHANNELS

- The buffered transfer mode
- Related signals
- Channels bus priority
- Data packing / unpacking
- Buffers chaining

THE FAST/GIGABIT ETHERNET CONTROLLER

- Frame format with and without VLAN option
- Ethernet controller organization
- PHY interface
- Hash table restrictions
- Buffer descriptors management
- Transmit sequence
- Receive sequence

TCP/IP ACCELERATION HARDWARE

- Checksum management
- TCP segmentation in the transmit path
- VLAN tagged frames

THE UARTS

- The UART frame : break, idle, start, stop
- Transmission and reception FIFOs use
- Flow control signals management

THE IIC PORTS

- IIC protocol basics
- Transfer timing diagrams
- Transmit and receive sequences

Renseignements pratiques

Duration : **5 days**
Cost : **2100 € HT**