



AT4 - AT91SAM3 series implementation

This course covers AT91SAM3S, AT91SAM3U and AT91SAM3N ARM-based MCU family

Objectives

- This course has 5 main objectives:
 - Describing the hardware implementation and highlighting the pitfalls
 - Describing the ARM Cortex-M3 core architecture
 - Becoming familiar with the IDE and low level programming
 - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
 - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex AT91SAM3 device, the AT91SAM3S4C.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.
 - According to the actual reference chosen by the customer, some chapters may be removed.
- Products and services offered by ACSYS:
 - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
 - ACSYS has also an expertise in FreeRTOS porting and uIP / LWIP stack or Interniche stack integration.

A lot of programming examples have been developed by ACSYS to help the attendee to become familiar with the IDE he has chosen. That is why the labs included in this course can be compiled and executed under 3 possible IDEs: IAR, Keil and GCC / Lauterbach Trace32.

A more detailed course description is available on request at training@ac6-training.com

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M3 core. Our course reference cours RM2 - Cortex-M3 implementation details the operation of this core.
- The following courses could be of interest:
 - USB Full Speed High Speed and USB On-The-Go, reference cours IP2 - USB 2.0
 - SD / MMC, reference cours IS2 - eMMC 5.0

Environnement du cours

- Cours théorique
 - Support de cours au format PDF (en anglais) et une version imprimée lors des sessions en présentiel
 - Cours dispensé via le système de visioconférence Teams (si à distance)
 - Le formateur répond aux questions des stagiaires en direct pendant la formation et fournit une assistance technique et pédagogique
- Au début de chaque demi-journée une période est réservée à une interaction avec les stagiaires pour s'assurer que le cours répond à leurs attentes et l'adapter si nécessaire

Audience visée

- Tout ingénieur ou technicien en systèmes embarqués possédant les prérequis ci-dessus.

Modalités d'évaluation

- Les prérequis indiqués ci-dessus sont évalués avant la formation par l'encadrement technique du stagiaire dans son entreprise, ou par le stagiaire lui-même dans le cas exceptionnel d'un stagiaire individuel.
- Les progrès des stagiaires sont évalués par des quizz proposés en fin des sections pour vérifier que les stagiaires ont assimilé les points présentés
- En fin de formation, une attestation et un certificat attestant que le stagiaire a suivi le cours avec succès.
 - En cas de problème dû à un manque de prérequis de la part du stagiaire, constaté lors de la formation, une formation différente ou complémentaire lui est proposée, en général pour conforter ses prérequis, en accord avec son responsable en entreprise le cas échéant.

Plan

ARCHITECTURE OF AT91SAM3 MCUs

- ARM core based architecture
- Description of AT91SAM3N, AT91SAM3U and AT91SAM3S SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AHB-to-APB bridge
- Integrated memories
- SoC mapping

THE ARM CORTEX-M3 CORE

- V7-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism
- Memory Protection Unit

BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 IDEs: Keil, IAR and GCC / Lauterbach.
- Thus the customer has just to indicate which one he has chosen.
 - Getting started with the IDE
 - Parameterizing the compiler / linker
 - Creating a project from scratch
 - C start program

PROGRAMMING AND DEBUGGING

- Debug architecture
- Programming

RESET, POWER AND CLOCKING

- Power control
- Reset controller
- Clocking
- Low power modes

INTERNAL INTERCONNECT

- Bus matrix
- Peripheral DMA Controller (PDC)
- DMA Controller (DMAC), AT91SAM3U

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module

INTEGRATED MEMORIES

- Embedded flash memory
- Internal SRAM
- Internal ROM

MEMORY INTERFACE

- High Speed MultiMedia Card Interface
- Static Memory Controller

TIMERS

- Timer counter
- PWM
- Real-time Timer
- Real-time Clock
- Watchdog timer

ANALOG MODULES

- 12-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- 12-bit Analog-to-Digital Converter, ADC12B, AT91SAM3U
- 12-bit Digital-to-Analog Converter
- Analog Comparator Controller

SECURITY AND INTEGRITY

- Cyclic Redundancy Check Calculation Unit
- Chip Identifier

CONNECTIVITY AND COMMUNICATION

- SPI
- Synchronous Serial Controller
- UART
- USART
- Two-Wire Interface
- USB Device FS
- USB Device HS, AT91SAM3U
- ISO7816 smartcard interface

Renseignements pratiques

Durée : 5 jours
Prix : 1950 € HT