ac6

IS3 - Serial ATA III

This course covers SATA III

Objectives

- This course explains how SATA maintains compatibility with IDE software management .
- The hardware layer is detailed, including the analog part and Out-Of-Band signals operation.
- The FIS is analyzed in order to understand the dialog between Host Controller and mass storage device.
- The course clarifies the programming interface specified by the Advanced Host Controller Interface .
- The Gen3 physical layer specification and testing requirements are particularly detailed.
- The course describes the low power modes.

- It has been delivered several times to companies developing SoCs for wireless / consumer market.

Timing diagrams are taken from a PC implementing a SATA interface thanks to the Lecroy analyser.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a serial bus like USB or Ethernet is recommended.

Course Environment

- Theoretical course
    - PDF course material (in English) supplemented by a printed version for face-to-face courses.
    - Online courses are dispensed using the Teams video-conferencing system.
    - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
    - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

ORIGINS OF THE SATA INTERFACE

- Parallel ATA limitations
- Faster HDD access and logical block addressing (LBA)
- ATAPI for support of other peripheral devices
- Programmed Input / output, direct memory access (UDMA)
- Revisions of the SATA specification
- Compatibility with SAS

SATA ARCHITECTURE

- Architectural layering
- Hot plugging
- Port multiplier
- Usage model description

PHYSICAL LAYER

- Cable and connectors
- Analog front end
- Electrical signalling
- Separate point-to-point AC-coupled LVDS links
- Spread Spectrum Clocking
- Elastic buffer
- Loopback mode
- Test pattern requirements
- Testing Gen3
- Jitter considerations
- Explaining the various tests used to qualify transmitter and receiver

OUT-OF BAND AND PHY POWER STATES

- COMRESET sequence
- COMINIT sequence
- COMWAKE sequence

LINK LAYER

- 8b/10b coding
- Scrambling
- Primitives description and utilization
- Arbitration sequence
- FIS flow control
- Transitions to low power modes

ATA REGISTERS

- PATA emulation
- Interrupt virtualization

TRANSPORT LAYER

- Introduction to FIS transfer
- Interaction with Command layer
- Retry protocol

PHY INTERFACE FOR SATA 3 (PIPE)

- Possible PIPE clocks and data bus widths
- Reset sequence
- Power management
- Changing signalling rate
- Error detection
- Loopback

ADVANCED HOST CONTROLLER INTERFACE (AHCI 1.3)

- System memory structures
- Native Command Queuing
- FIS-based switching
- Command completion coalescing
- Power management
- Interrupt management
- Data transfer operation
- Error reporting

COMMANDS

- ATA-8 command set
- Reset protocol, diagnostic protocol, PIO protocol, DMA protocol, PACKET protocol
- First party DMA
- Boot sequence capture and analyzis

Renseignements pratiques

Duration : 2 days
Cost : 1880 € HT