IS5 - SD UHS II (Ultra High Speed II)

This course covers UHS-II which is the enhanced version of SD

Objectives

- This course explains how legacy SD commands are transported over UHS II.
- The hardware layer is detailed, including the analog part.
- The link layer operation is explained through sequences clarifying flow control and acknowledgement mechanisms.
- The course describes the low power modes.
- The enumeration and configuration for a point-to-point or ring topology is studied.
- Data protection system is also covered.

- This training has been delivered several times to companies developing SoCs for wireless / consumer market.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of mass-storage interface, such as SD/MMC or USB mass storage class is recommended.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

OVERVIEW

- Description of a NAND flash
- Connection topologies
- Interface speed
- Protocol layers
- Transactions

PHYSICAL LAYER

- Range definition for data rates
- Impedance and termination scheme
- Line states
- 8b10b coding scheme
- Control symbols
- Test modes, loopback

LINK LAYER

- Packet framing
- Message packets
- Physical Lane State Machine
- Data Link State Machine
- Power management
- Flow control
- Data integrity
- Scrambling
- Boot code loading

PHY-LINK INTERFACE

- Interface signals
- Clock generation
- Timing diagrams

COMMON TRANSACTION LAYER

- Packet formats
- Transition to Dormant mode
- Device initialization
- Enumeration
- Configuration
- Registers mapping and description
- Timing rules

SD TRANSACTION LAYER

- Summary of legacy SD commands
- Transaction Control and Management state machine
- Basic transaction rules
- Error handling

DATA PROTECTION SYSTEM

- System and user password
- Encryption key

- DPS command set

Renseignements pratiques

Duration : 2 days
Cost : 1970 € HT