Training CYCLONE-V CORTEX-A9 HARD PROCESSOR SYSTEM: This course covers the hard IPs present in Cyclone-V Intel (Altera) FPGA family, based on ARM Cortex-A9 CPU - Programming: Logique Programmable

This course covers the hard IPs present in Cyclone-V Intel (Altera) FPGA family, based on ARM Cortex-A9 CPU

Objectives

- This course aims to clarify the Cyclone-V Cortex-A9 Hard Processor System.
- The interconnect based on ARM NIC-301 is particularly detailed.
- Hardware implementation of the Cortex-A9 is described, including reset and clocking.
- The possible boot sequences, involving or not the FPGA configuration, are explained.
- Interaction between level 1 caches, level 2 cache and main memory is studied through sequences.
- MMU operation is described.
- Spin-lock implementation in a multicore system is also detailed.
- The exception mechanism is explained, focusing on Cyclone-V interrupt mapping.
- An overview of the Coresight specification is provided prior to describing the debug related units and general Cyclone-V debug infrastructure, involving both the Hard Processor System and the FPGA portion.
- The operation of the Snoop Control Unit when supporting SMP is fully explained, particularly the utilization of cache tag mirrors, the advantage of connecting DMA channels to ACP and the sequences that have to be used to modify a page descriptor.
- Integrated SDRAM and Flash controllers, which can be accessed by FPGA masters and processor block masters, are fully described.
- Integrated peripherals are studied, especially the gigabit Ethernet MACs and the USB2.0 OTG controllers.

- Products and services offered by ACSYS:
  - AC6 is able to assist the customer by providing consultancies. Typical expertises are done during system architecture definition, software debugging, performance tuning.
  - Note that AC6 has a long experience with processor implementation in civil avionics systems.

Labs included in this course are compiled with RVDS 4.1 and executed under Lauterbach Trace32.
A more detailed course description is available on request at training@ac6-training.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-A9 core. Our course reference RA2 - Cortex-A9 implementation course details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0 course
  - Ethernet and switching, reference N1 - Ethernet and switching course
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocol course
  - CAN bus, reference IA1 - CAN bus course
  - SD / MMC, reference IS2 - eMMC 5.0 course
  - PCI Express, reference IC4 - PCI Express 3.0 course

Plan

First day

INTRODUCTION TO CORTEX-A9

- Block diagram, 1 or 2 AXI master interfaces
- Instantiated options

CYCLONE-V OVERVIEW

- Hard Processor System block diagram
- FPGA portion
- Possible boot scenario
- HPS-FPGA interfaces
- Address mappings, translation when implementing ACP

CLOCK AND RESET MANAGERS

- Reset sources
- Hardware sequenced resets
- Block diagram, integrated three PLLs
- Main clock group

BOOTING AND CONFIGURATION

- Boot sequence
- Selecting the interface from which the boot code will be loaded
- Initial software, boot loader
- Independent HPS booting and FPGA configuration

AMBA 4

- AXI
  - Separate address/control and data phases
  - AXI channels, channel handshake
  - Transaction ordering, out of order transaction completion
  - Read and write burst timing diagrams
  - Cortex-A9 external memory interface, ID encoding
  - NIC-301 AXI interconnect
- APB 3

MEMORY MANAGEMENT UNIT

- MMU objectives
- Page sizes
- Address translation
- Utilization of memory barrier instructions
- Format of the external page descriptor table
- TLB organization
- TLB lockdown
- Abort exception, on-demand page mechanism
- MMU maintenance operations

- Using a common page descriptor table in an SMP platform, maintaining coherency of multiple TLBs

Second day

LEVEL 1 MEMORY SYSTEM

- Cache organization
- Supported maintenance operations
- Write-back write allocate cache allocation
- Memory hint instructions PLD, PLI, PLDW, data prefetching

HARDWARE COHERENCY

- Snooping basics
- Snoop Control Unit: cache-to-cache transfers
- MOESI state machine
- Understanding through sequences how data coherency is maintained between L2 memory and L1 caches
- Accelerator Coherency Port: connecting a DMA channel that uses this port to enforce coherency of data it is transmitting

PL310 LEVEL 2 CACHE

- Cache configurability
- AXI interface characteristics
- Understanding through sequences how cacheable information is copied from memory to level 1 and level 2 caches
- Transient operations, utilization of line buffers LFBs, LRBs, EBs and STBs
- Cache event monitoring
- Describing each maintenance operation
- Cache lockdown
- Initialization sequence

SYSTEM INTERCONNECT

- Interconnect block diagram
- Bridge to APB, L4 slaves
- L3 main switch
- QoS, arbitration policies
- Cyclic dependencies avoidance schemes
- ACP ID mapper
- HPS-to-FPGA AXI bridge
- FPGA-to-HPS AXI bridge
- Clarifying the conditions for an FPGA IP to use hardware coherency

Third day

MEMORY CONTROLLERS

- On Chip RAM
- Integrated DDR3 controller
  - Introduction to DDR3
  - Parameterizing the controller according to DDR3 device timings
  - FPGA-to-HPS SDRAM port utilization, 64-, 128- or 256-bit Avalon or AXI ports
  - Multiport scheduling
- NAND flash controller
  - Discovery and initialization

- Data DMA
- ECC control
- SD/MMC controller
  - Card detection and initialization
  - Integrated descriptor-based DMA
  - 4-KB data FIFO
- Quad SPI flash controller
  - Direct access and indirect access modes
  - XIP flash device
  - STIG operation

CORTEX-A9 HARDWARE IMPLEMENTATION

- Clock domains
- Reset domains
- Power control, dynamic power management
- Wait For Interrupt architecture
- AXI master interface attributes
- Level 2 memory interface: AXI read & write issuing capability

INTERRUPT CONTROLLER

- Cortex-A9 exception management
- Cyclone-V interrupt mapping
- Integrated timer and watchdog unit in MPCore
- Interrupt groups: STI, PPI, SPI, LSPI
- Prioritization of the interrupt sources

Fourth day

CORESIGHT DEBUG UNITS

- Invasive debug, non-invasive debug, taking into account the secure attribute
- APBv3 debug interface
- Connection to the Debug Access Port
- Debug facilities offered by Cortex-A9
- Process related breakpoint and watchpoint
- Event catching
- Debug Communication Channel
- PTM interface, connection to funnel
- Cross-Trigger Interface, debugging a multi-core SoC
- Generating debug events from / to the FPGA fabric
- Cyclone-V debug infrastructure
- System Trace Macrocell
- Embedded Trace Router
- SCAN manager

GPIO

- Pin direction configuration
- Configurable interrupt mode

FPGA MANAGER

- Managing and monitoring the FPGA portion
- Handshaking inputs when booting from FPGA

- Generating interrupts based on changes in the FPGA portion
- Resetting the FPGA portion
- FPGA configuration, partial reconfiguration, MSEL pins

SYSTEM MANAGER

- Selecting EMAC PHY interfaces
- Selecting SD/MMC controller clock options
- Connecting CAN controllers to DMA channels
- Managing parity errors detected in HPS, injecting errors
- Providing the boot ROM code with boot information required to support HPS boot
- Selecting NAND flash controller boot options
- Configuring the USB controller

DMA CONTROLLER

- 8 logical channels, arbitration
- Scatter / gather, list of descriptors
- DMA instruction execution engine, variable-length instructions, instruction set description
- Multi-FIFO operation
- Interrupt management
- Using an event to restart a DMA channel

Fifth day

ETHERNET MACS

- Ethernet basics
- PHY connection, PHY management interface
- Incoming frame filtering mechanisms, hash tables
- Flow control in full duplex mode
- VLAN support
- TCP-IP offload
- Audio video (AV) feature
- IEEE1588 protocol support

USB 2.0 OTG CONTROLLER

- Connecting the PHY
- Explaining what is OTG, SRP and HNP
- High-speed operation
- Host operation, muxing periodic and non-periodic traffics

LOW SPEED SERIAL INTERFACES

- Synchronous Serial Port
- I2C interfaces
- UART
- CAN

HPS CORE INSTANTIATION

- Configuring FPGA interfaces
- Configuring HPS clocks
- Configuring the external memory interface
- Generating the HPS core

Renseignements pratiques

Duration : 5 days
Cost : 2550 € HT