H6 - Lattice - PCIe 1.1 x1, x4 IP core

This course describes the implementation of the Lattice PCIe core present in ECP2M, ECP3 and SCM FPGA families

Objectives

- Clarifying the architecture of the PCIe core, distinguishing soft IPs from hard IPs (e.g. the Serdes) .
- Developing software to drive the core and achieve desired functionality.
- Highlighting the management of transmit credits through examples.
- Understanding the various parameters that have to be defined in IPexpress GUI.

- This course is delivered by Ac6 engineers, expert on PCIe, who has also developed trainings on PCIe core for Xilinx.

Lattice software (ispLEVER) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of PCI Express 1.1 is recommended, see our course reference I3.
- Experience with Lattice ispLEVER IDE is recommended, see our course reference H2.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

DAY 1

INTRODUCTION TO LATTICE PCIe CORE

- Core versions.
- Core requirements, data bus width, performance, resource utilization.
- Indicating how each PCIe protocol layer is implemented and what has to be done in the user logic.
- Interfaces.

CLOCK AND RESET INTERFACE

- 125-MHz and 250-MHz clock domains.
- LatticeECP3 and LatticeECP2M PCIe clocking scheme.
- LatticeSCM PCIe clocking scheme.
- PCIe power-up.

TRANSMIT AND RECEIVE TLP INTERFACE

- Understanding the ports of the transmit interface.
- Nullifying a TLP being transmitted.
- Checking transmit credits prior to send Non-Posted, Posted or Completion packets.
- Completion read boundary definition.
- Understanding the ports of the receive interface.
- Transaction layer error detection and management, generating error messages.
- Updating transmit credits for the peer device.
- Address decode logic in the receiver, BAR registers.
- Completion time-out detection.
- ECRC checking and generation.
- Providing the header of a mal-formed packet detected by the user logic.

PHYSICAL LAYER INTERFACE

- Describing all states and transitions of the PCIe LTSSM.
- Signal description.
- Tracking the state of the LTSSM.
- Forcing the transition to specified states, in order to accelerate simulations.
- Multi-lane operation.
- Adapter card concerns.
- MultiChannel Adapter (MCA), LatticeSCM reference design.

DAY2

LINK LAYER INTERFACE

- Describing the APSSM state machine used to control the power states of the link and of the function.
- Getting the state of the link layer.
- Transmitting power messages.
- Receiving power messages.

CONFIGURATION REGISTERS

- Ports used to export the configuration value set by the host firmware.
- Ports used to force the contents of some registers.

- Detailing all registers, type 0 header, PCIe-related registers, power-management related registers, MSI relared registers, advanced error reporting related registers, and serial number register.
- Getting the device ID, necessary to respond to configuration requests.

INTERRUPT AND MSI

- Explaining the disadvantages of legacy interrupts.
- Generating an interrupt assert / deassert message.
- Determining whether the host software supports MSIs.
- Selecting an MSI number and generating the MSI.
- Behavior of the back end logic when the host software allocates less MSIs than requested.

WISHBONE INTERFACE

- Transfer protocol basics.
- Accessing the registers of the configuration space.
- Wishbone interface memory map.
- Description of IP control and status registers.

IP CORE IMPLEMENTATION

- Lattice SCM MACO blocks.
- Creating the IP through IPexpress GUI, explaining each parameter that has to be defined by the user.
- Implementing loopback.
- Total EBR count based on Max TLP size.
- Created files and directories.
- Simulation strategies.
- LatticeECP3 and LatticeECP2M PIPE Simulation.
- Locating the IP.
- Setting Design Constraints.

SCATTER-GATHER DMA CONTROLLER IP CORE

- Device support for SGDMAC core v2.1.
- Scatter-gather DMA principle.
- Arbitration between channels.
- DMA engine.
- System configurations, utilization in a PCIe design to fill / empty transmit / receive FIFOs.

Renseignements pratiques

Duration : 2 days
Cost : 1350 € HT