Training Programmable component fundamentals: This training is intended to professional who want to use or maintain programmable components - Programming: Logique Programmable

V0 - Programmable component fundamentals

This training is intended to professional who want to use or maintain programmable components

Objectives

- Knowing the programmable logic basics
- Knowing the general offer for CPLDs and FPGAs
- Understand application description in HDL
- Understand the logical synthesis notions and process flow
- Discover FPGA programming in VHDL and Verilog
- Understand how to elaborate and simulate a design

Course environment

- A PC in pairs
- Xilinx ISE Design Suite 14.4 Webpack Edition
- A Nexys-3 (Xilinx Spartan6-based) board

Prerequisites

- Knowledge of digital technology
- Concepts of Boolean algebra
- Some programming concepts are desirable (whatever language)

Plan

First Day

From the logic gate to the CPLDs and FPGAs

- Reminder on digital electronic
- Structure of an Integrated Circuit
- SSI (small scale integration), TTL
- MSI (medium scale integration), PALs, GALs, PLDs
- LSI (large scale integration), CPLDs
- VLSI (very large scale integration), ASICs, ASSPs, FPGAs
- Logical architectures evolution
- The various components
- Technologies available on the market

- Technology constraints
- Interconnection methods (SRAM, Fuse, AntiFuse, Flash)
- Clock distribution
- Logic element types
- Timing issues

HDL Contribution

- Interest of HDL programming
  - VHDL
  - Verilog
- Different steps of the design
  - Programming
  - Simulation
  - Synthesis
  - Mapping
  - Place and Route
  - Timing Analysis
  - Bitstream generation
- Definition of a project
- Structure of a program
- Allocation of PIN-OUT
- Programming

Exercice: *Understanding the steps of design and programming:*

- *Getting started with the ISE IDE*
- *Creating a project from scratch*
- *Synthesis, Translate*
- *Map*
- *Place and Route (PAR)*
- *BitGen*
- *Report Analysis*
- *Assigning I/O locations using Planahead (editing constraint file)*
- *Schematics*
- *Analyzing the placement*
- *Flashing with Impact*

Second Day

Schematic Editor

- The schematic capture
- Primitives and symbols definition
- Resources definition
- Compilation

Exercice: *Developing a new IP with the Schematic Editor, Designing a Bound Detector*

HDL Basic Concepts (VHDL and Verilog)

- Entity/ Architecture and Module
- Signals and wires
- Processes and Always/Initial statements
- Connecting existing IPs together

Exercice: *Adding a 7-Segment Display to your design*

Test benches and simulation

- HDL instructions specific to simulation
- Functional and behavioral simulation (with delays)
- Test vector generation

Exercice: *Getting started with the ISIM simulator, developing a tesbench and simulating the previous designs*

Renseignements pratiques

Duration : 2 days
Cost : 1710 € HT