FF3 - MCF532X implementation

This course covers MCF532X ColdFire MCUs, for instance the MCF5329

Objectives

- The course details the low level programming of the V3 core.
- An example of SDRAM controller initialization is provided.
- Interfacing with external devices is explained.
- The interrupt controller is viewed in detail.
- DMA transfers terminated by interrupt is studied.
- A programming example has been developped for each internal peripheral (USB, CAN, serial, I2C, timer).
- The course details the various operating modes supported by the Fast Ethernet Controller, particularly the frame filtering logic.

- This course has been delivered several times to companies developing industrial and medical equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as Fast Ethernet.

- *They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.*

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- USB 2.0, reference IP2 - USB 2.0course
- CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented

- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO MCF532X

Overview

- Differences between ColdFires and 68K processors
- 5329 block diagram, differences between 5327, 5328 and 5329
- Internal data paths
- Crossbar switch module
- Memory mapped I/O organization

PROCESSOR CORE

V3 CORE

- V3 core pipeline
- Addressing modes
- Branch instructions
- Data transfer instructions
- Mac instructions
- Control instructions
- Stack management, subroutine call and return
- C to assembly interface, organization of the stack frame
- Exception management : vector table, priority, masking
- Internal SRAM
- Cache basics
- Cache operation, software control
- V3 core pipeline
- Addressing modes
- Branch instructions
- Data transfer instructions
- Mac instructions
- Control instructions
- Stack management, subroutine call and return
- C to assembly interface, organization of the stack frame
- Exception management : vector table, priority, masking
- Internal SRAM
- Cache basics
- Cache operation, software control
- Debug facilities

PLATFORM

HARDWARE IMPLEMENTATION

- Clocking, power management
- Chip configuration module
- Reset control module
- System control module
- Real Time Clock

- Flexbus
- Data transfer sequence
- Burst cycles
- Bus error management
- General Purpose Input / Output module
- DRAM / SDRAM basics
- The 532X SDRAM controller

INTERRUPT CONTROLLERS AND TIMER MODULES

- Vectorized vs auto-vectorized mode
- Interrupt processing sequence
- Prioritization between interrupt controllers
- Low power wake-up operation
- The software watchdog
- Edge port module
- PWM module
- Programmable interrupt timer modules
- DMA timers

THE eDMA CONTROLLER

- EDMA microarchitecture
- Initialization
- Channel linking
- Transfer error management

INTEGRATED I/Os

LIQUID CRYSTAL DISPLAY CONTROLLER

- LCD screen format
- Graphic window on screen
- Display data mapping
- Black-and-White operation
- Color generation
- Frame Rate modulation control

COMMUNICATION CONTROLLERS

- The UART Module
- The SSI,
- The QSPI,
- The I2C controller
- The FlexCAN controller
- The Fast Ethernet Controller, Ethernet basics, addressing, frame format, clock recovery, MII hardware interface, auto-negociation, buffer management, buffer chaining, address filtering, use of hash tables, full duplex operation, flow control, receive and transmit sequences, error management
- The USB Host module, USB basics, EHCI specification, functional description
- The USB On-The-Go module, ULPI interface, connection of an external PHY, device data structures, device operational model, deviations from the EHCI specification

CRYPTOGRAPHY MODULES

- Message Digest Hardware Accelerator
- Random Number Generation
- Symmetric key hardware accelerator, introduction to data encryption standards
- Data flow, management of input and output FIFOs
- Algorithms : AES, DES, 3DES

- Cipher modes : ECB, CBC, CTR

Renseignements pratiques

Duration : 4 days
Cost : 1950 € HT