FCQ9 - T2081 QorIQ implementation

This course covers NXP QorIQs T2080 & T2081

Objectives

- **This course has the following objectives:**
  - **Describing the hardware implementation, particularly the boot sequence and the DDR3 controller**
  - **Understanding the features of the internal interconnect and related units and mechanisms such as PAMU, CPC and stashing**
  - **Explaining the standard bus interface controllers, PCIe, USB, SATA and MMC-SD**
  - **Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units**
  - **Clarifying the operation of the Datapath Acceleration Architecture that assists the processor core in taking in charge buffer allocation, queue management, frame management and particularly incoming frame classification, pattern searching, and encryption**
  - **Describing the various debug units and their utilization to fix errors in a multicore / multimaster SoC.**

A more detailed course description is available on request at training@ac6-training.com
This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Pre-requisites and related courses

- **Experience of a 32-bit processor or DSP is mandatory.**
- **Note that the e6500 Power core is covered in a separate course reference FCC4 - e6500 implementationcourse.**
- **The following courses could also be useful:**
  - **PCIe IC4 - PCI Express 3.0course**
  - **Ethernet N1 - Ethernet and switchingcourse**
  - **USB 2.0 IP2 - USB 2.0course**
  - **SATA IS3 - Serial ATA IIIcourse**

Plan

T2081 ARCHITECTURE

OVERVIEW

- **Differences between T2080 and T2081**
- **CoreNet coherency fabric**
- **Coherency subdomains**
- **Memory map, local access windows**
- **Highlighting data paths inside the T2081**
- **e6500 core integration**

SOC PLATFORM

POWER, RESET AND CLOCKING

- • Configuration signals sampled at reset
- Pre-boot loader, initializing the platform prior to starting the processor core
- PCIe configuration
- Boot memory space, boot space translation
- Clocking, system clock domains
- SerDes high speed lanes configuration
- Advanced power management

SECURE BOOT

- Objectives of trust architecture
- Internal boot ROM, secure boot sequence
- Code signing
- External tamper detection
- Run time integrity checker

CORENET PLATFORM CACHE

- Entry locking
- Operation as memory-mapped SRAM
- Partitioning between coherency domains
- Stashing

PERIPHERAL ACCESS MANAGEMENT UNIT (PAMU)

- Controlling master access permissions through Logical I/O Device Number
- Operation mode translation
- Steps in processing of DSA operations by PAMU
- PAMU gate closed state

MULTIPROCESSOR PERIPHERAL INTERRUPT CONTROLLER

- Interrupt nesting
- Description of the 4 timers / counters
- e6500-to-e6500 interrupt capability

LOW SPEED PERIPHERALS

- Description of the NS16452/16552 compliant Uarts
- I2C controller
- eSPI controller

ENHANCED SDHC

- Transfer protocol, single block, multiple block read and write
- Internal and external DMA capabilities
- SD protocol unit
- Card insertion and removal detection

USB CONTROLLERS

- Host or device support

- **EHCI support, scheduling the various transactions into frames**
- **Integrated PHY**
- **Endpoint configuration**
- **Device operation**

HARDWARE IMPLEMENTATION

THE DDR3 / 3L MEMORY CONTROLLER

- **Jedec specification basics**
- **DDR3 fly-by architecture, write leveling**
- **Reset sequence, dynamic ODT, ZQ calibration**
- **Bank activation, read, write and precharge timing diagrams, page mode**
- **Initial configuration following Power-on-Reset**
- **Timing parameters programming**
- **Initialization routine**
- **Tuning the performance of the DDR3 controller**
- **Testing the memory using patterns**

INTEGRATED FLASH CONTROLLER

- **Functional muxing of pins between NAND, NOR, and GPCM**
- **Data Buffer Control**
- **Normal GPCM FSM**
- **NOR flash FSM**
- **NAND flash FSM**
- **Boot from NAND**

INTEGRATED DMA CONTROLLERS

- **Priority between the 4 channels**
- **Support for cascading descriptor chains**
- **Scatter / gathering**

PCI EXPRESS INTERFACE

- **Acting as a bridge when Root Complex**
- **Transaction ordering rules**
- **Programming inbound and outbound ATMUs**
- **Benefits of MSIs**
- **Configuration, initialization**
- **SR-IOV implementation, Alternative Routing ID**

SERIAL RAPIDIO INTERFACE

- **RapidIO port**
- **Accept-all mode of operation**
- **RapidIO doorbell and port-write unit**
- **Accessing configuration registers via RapidIO packets**
- **Programming inbound and outbound ATMUs**

SATA CONTROLLERS

- **SATA basics**
- **Support for SATA II extensions**
- **Electrical specification**
- **Bringing the SATA controller online/offline**

- **Native command queuing, command descriptor**

DATAPATH PROCESSING SUBSYSTEM

DPAA OVERVIEW

- **Definitions: buffer, buffer pool, frame, frame queue, work queue, channel**
- **Frame formats**
- **DPAA Configuration and Initialization**

QUEUE MANAGER

- **Objectives if this accelerator**
- **Frame description**
- **Frame queue descriptor, frame queue descriptor cache**
- **Frame queue state machine**
- **Work queues and channels**
- **Enqueue and dequeue portals**
- **Sequences to understand how frames a enqueued / dequeued**
- **Class and intra-class scheduling rules**
- **Stash transaction flow control and scheduling**
- **Congestion avoidance**
- **Order definition point implementation**
- **Traffic shaping through CEETM**

BUFFER MANAGER

- **Objectives if this accelerator**
- **Central resource pool management function**
- **External linked list LIFO**
- **Direct connect portals**
- **Buffer Pool State Change Notifications**

FRAME MANAGER

- **Objectives if this accelerator, parsing, classifying and distributing in-line/off-line packet**
  - **Rx BMI features**
  - **Tx BMI features**
  - **Offline parsing, host command features**
  - **Frame processing manager**
  - **FMan controller**
  - **Host commands**
  - **Parser**
  - **Key generator**
  - **Policer**
- **New features:**
  - **IP fragmentation / re-assembly**
  - **Header manipulation**
  - **Autonomous 802.1qaz**
  - **Data center bridging**
  - **Ingress multicast**

MULTI-RATE ETHERNET MAC (mEMAC)

- **Physical interfaces**
- **MAC address recognition**
- **Accessing PHY registers, clause 45**

- **Priority Flow Control**
- **RMON statistic counters, carry registers**

RAPIDIO MESSAGE MANAGER

- **2 inbox/outbox mailboxes (queues) for data and one doorbell message structure**
- **Multicasting**
- **Outbound segmentation units**

SECURITY ENGINE

- **Introduction to DES, 3DES and AES algorithms**
- **Job management using QMan interface**
- **Job descriptor parsing**
- **Sharing descriptors**
- **Selecting the authentication / cryptographic algorithm**
- **Run Time Integrity Checking**
- **Public Key Hardware Accelerator (PKHA)**
- **SNOW 3G Accelerator**
- **Data Encryption Standard Accelerator (DES)**
- **Cyclic Redundancy Check Accelerator (CRCA)**
- **Message Digest Hardware Accelerator (MDHA)**
- **Elliptic Curve Cryptographic Functions**

PATTERN MATCHER

- **Objective of this unit, identifying signatures in incoming gigabit streams**
- **Connection to QMan and BMan**
- **Support for wildcarding with no pattern explosion**
- **Updating the pattern database**
- **Definition of a regular expression**
- **Pattern Matcher Frame Agent**
- **Pattern description block caching**
- **Key Element Scanner, trigger stage, confidence stage**
- **Data Examination Engine**
- **Stateful Rule Engine, Stateful Rule Physical Structure, SRE instruction set**

GLOBAL FUNCTIONS, DEVELOPMENT AND DEBUG

PERFORMANCE MONITOR AND DEBUG FEATURES

- **NEXUS Aurora link**
- **Event processing unit**
- **Chaining, triggering**
- **Watchpoint facility**
- **Trace buffer**
- **Cross-Functional Debug Components**
- **CoreNet debug**
- **OCeaN debug**

Renseignements pratiques

Duration : 5 days
Cost : 2930 € HT