FPQD - MPC8572E implementation

This course covers PowerQUICC III MPC8572E dual core device

Objectives

- The course details the Ocean crossbar operation.
- Cache coherency protocol is introduced in increasing depth and the benefit of data stashing is explained.
- The e500 core is viewed in detail, especially the SPU that enables Floating point and vector processing.
- The boot sequence and clocking are explained.
- The course details the hardware implementation of the MPC8572E.
- A long introduction to DDR2/3 SDRAM operation is done before studying the DDR SDRAM controller.
- An in-depth description of the RapidIO port and the PCI-Express port is done.
- The course highlights both hardware and software implementation of gigabit / fast / Ethernet controllers.
- The course clarifies the operation of hardware acceleration mechanisms : Gigabit Ethernet TCP/IP offload engine, Pattern matcher and Table Lookup Unit.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
  - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
  - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
  - for any information contact training@ac6-training.com

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- Experience of a 32 bit processor or DSP is mandatory.
- The knowledge of the following interconnect standards may be required:
  - RapidIO see our course reference IC5 - RapidIO 3.0course
  - PCI Express, see our course reference IC4 - PCI Express 3.0course
  - Gigabit Ethernet, see our course reference N1 - Ethernet and switchingcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.

- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO MPC8572E

Overview

- Internal data flows, OCEAN switch fabric, packet reordering
- Implementation examples
- Address map, ATMU, OCEAN configuration
- Local vs external address spaces, inbound and outbound address decoding

THE e500 CORES

THE INSTRUCTION PIPELINE

- Dual-issue superscalar control
- Dynamic branch prediction
- Execution timing

DATA AND INSTRUCTION PATHS

- Load store unit
- The LMQ
- Store miss merging and store gathering
- Memory access ordering

THE MEMORY MANAGEMENT UNITS

- Thread vs process
- The first level MMU and the second level MMU
- Snooping of TLBs
- TLB software reload
- Process protection, variable number of PID registers and sharing
- 36-bit real addressing

CACHES

- The L1 caches
- Cache coherency
- Level 2 cache
- Stashing mechanism

PROGRAMMING

- Differences between the new Book E architecture and the classic PowerPC architecture
- Signal Processing APU (SPU)
- PowerPC EABI : sections

EXCEPTIONS

- Book E exception handling
- Critical versus non critical
- Handler table
- Core timers

DEBUGGING

- Performance monitoring
- JTAG emulation
- Watchpoint logic

INFRASTRUCTURE

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- Power-on reset sequence
- Power-on reset configuration
- Boot page translation

DDR2/DDR3 SDRAM MEMORY CONTROLLER

- DDR2 and DDR3 Jedec specification
- On-Die termination
- Calibration mechanism
- Mode registers initialization, bank selection and precharge
- ECC error correction
- Address decode
- Timing parameters programming

LOCAL BUS CONTROLLER

- Multiplexed or non-multiplexed address and data buses
- Dynamic bus sizing
- GPCM, UPMs
- NAND flash controller

SERIAL RapidIO INTERFACE

- RapidIO port
- Message Unit
- Programming inbound and outbound ATMUs
- Hot-swap support
- Error handling

PCI EXPRESS INTERFACE

- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Configuration, initialization

PROGRAMMABLE INTERRUPT CONTROLLER

- Mixed mode vs pass-through mode
- Interrupt sources

- Understanding interrupt masking
- Interprocessor interrupts
- Nesting implementation

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Scatter / gathering
- Selectable hardware enforced coherency
- Ability to start DMA from external 3-pin interface

PATTERN MATCHER

- Objective of this unit
- Updating the pattern database
- Detecting patterns across packet boundaries
- Deflate engine

TABLE LOOKUP UNIT

- Exact match vs Longest prefix match
- Utilization in IPv6
- How software interact with the TLU unit

PERFORMANCE MONITOR AND DEBUG FEATURES

- Event counting
- Threshold events
- Watchpoint facility
- Trace buffer

INPUTS/OUTPUTS

THE ETHERNET CONTROLLERS

- Address recognition, pattern matching
- Buffer descriptors management
- Physical interfaces : GMII, MII, TBI or RGMII
- Layer 2 acceleration accept or reject on address or pattern match
- Direct queuing of four flows
- Management of VLAN tags and priority
- Quality of service
- IEEE1588 compliant time-stamping
- FIFO mode
- 10/100 Fast Ethernet Controller
- Buffer management
- MII interface

SECURITY ENGINE

- Overview of the encryption mechanism
- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- XOR acceleration

LOW SPEED PERIPHERALS

- Description of the NS16552 compliant Uarts

- Flow control signal management
- FIFO mode
- I2C protocol fundamentals
- Transmit and receive sequence
- GPIO configuration

Renseignements pratiques

Duration : 5 days
Cost : 2100 € HT