ac6

MV1 - MARVELL MV6446X implementation

This course covers Marvell Discovery III devices

Objectives

- The course describes the MV6446X internal data paths.
- The course explains how the host PowerPC and a CPU connected to PCI-X can synchronize to each other through the message unit.
- A long introduction to DDR SDRAM is done prior to describe the DDR SDRAM controller operation.
- The course focuses on the hardware implementation of the DDR SDRAM.
- The training explains how to implement chained DMA transfers, by using either IDMA channels or XOR engines.
- The course highlights the possible optimizations that can be implemented to boost the performance of the Ethernet controller.

- This course has been delivered several times to companies developing defence and avionics systems.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of PowerPC 60X / MPX bus. See our courses on NXP and IBM Microelectronics PowerPCs.

Related courses

- Ethernet and switching, reference <u>N1 - Ethernet and switching</u>course
- PCI, reference <u>IC1 - PCI 3.0</u>course
- PCI-X, reference <u>IC3 - PCI-X 2.0</u>course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

OVERVIEW

- 5-bus architecture, organization of a board based on MV6446X
- Frequency domains, fast path between CPU and SRAM / SDRAM
- Data integrity checking
- Internal crossbar
- Headers retarget

CPU INTERFACE

- CPU address space decoding
- CPU-to-PCI address remapping
- Arbitration, multi-processor operation
- Cache coherency
- Transaction ordering
- Hardware implementation

INTEGRATED SRAM

- Functional description, SRAM access arbitration
- Write-Through vs CopyBack coherency
- ECC protection

DDR INTERFACE

- Introduction to DDR SDRAM from Jedec specification
- Initialization sequence
- Page management
- Read and write transactions
- Transaction ordering
- Cache coherency
- ECC and read-modify-write transactions
- Hardware implementation, SSTL technology

DEVICE CONTROLLER

- Functional description, transaction queue, read and write data buffers
- Connecting 8/16/32 bit devices
- Timing parameters
- External acknowledgement
- Pack / unpack and burst support

PCI INTERFACE

- PCI bus arbitration
- Master operation in PCI and PCI-X mode
- Target operation in PCI and PCI-X mode
- PCI-to-PCI configuration transactions
- Address decoding
- Cache coherency
- Messaging unit

GENERAL PURPOSE INPUT/ OUTPUT PINS

- Pin direction and polarity definition
- Interrupt request inputs

- Multi Purpose Pin multiplexing

INTERRUPT CONTROLLERS AND TIMERS

- Watchdog timer
- Timers / counters
- Interrupt controller functional description

TWSI CONTROLLER AND RESET

- Master and slave operation, 7- or 10-bit addressing
- Master write sequence, master read sequence
- Slave write sequence, slave read sequence
- Reset pins and configuration
- Serial ROM initialisation
- Requirement for an external Central Resource CPLD

IDMA CHANNELS

- IDMA address decoding
- Demand mode
- Normal mode vs chained mode
- Channel activation

XOR ENGINES

- State machine : Active, Inactive and Paused states
- XOR, CRC and DMA operation modes, format of transfer descriptors
- Memory Initialization operation mode
- ECC error cleanup operation mode
- Address decode windows
- Address override capability
- Cache coherency

MULTI-PROTOCOL SERIAL CONTROLLERS

- Address decoding
- Pinout, connection to MPP logic
- Baud Rate Generator
- MPSC clocking
- SDMA operation
- Transmit descriptor format, ring organization
- Receive descriptor format, ring organization
- HDLC mode, UART mode, Transparent mode

GIGABIT ETHERNET CONTROLLERS

- Interface to the PHY
- Dedicated DMA
- Transmit weighted round-robin arbitration
- Backpressure mode
- Transmit and receive sequences
- Management interface
- MIB
- Synchronous FIFO interface
- DMA operation

Renseignements pratiques

Inquiry : 4 days