

## N3 - Ethernet 10 Gigabit

This course covers IEEE802.3 Ethernet 10 gigabit and SFP+

### OBJECTIVES

- ▶ This course explains the theory of Ethernet 10 Gigabit from IEEE802.3 standard.
- ▶ Implementation examples are provided for MAC and PHY.
- ▶ The hardware interfaces are fully detailed: XGMII, XAUI, XSBI and XFP+.
- ▶ The course describes the purpose of each unit present in the transmit and receive path.
- ▶ Software aspects, such as 10GBASE-T autonegotiation and more generally registers implemented in PHY sublayers are also covered.
- ▶ The course details the implementation of 10G Ethernet for backplanes, clarifying 10GBASE-KR FEC, training and autonegotiation.

*A more detailed course description is available on request at [training@ac6-training.com](mailto:training@ac6-training.com)*

### PREREQUISITES

- ▶ Knowledge of gigabit Ethernet, see our course: Ethernet and switching, reference [N1 - Ethernet and switching](#) course

### Plan

#### INTRODUCTION TO ETHERNET 10G

- ▶ Clarifying the various types of Ethernet 10G PHYs
- ▶ Maintaining backwards compatibility with Ethernet 10/100/1000 Mbps
- ▶ Full duplex only operation

#### MAC / PHY INTERFACE

- ▶ MAC frame assembly
- ▶ XGMII transfer protocol, the 4 Bytes lanes
- ▶ XAUI electrical interface, delay constraints

#### MANAGEMENT INTERFACE

- ▶ Extension to this Clause 22 specification
- ▶ MDIO Manageable Device
- ▶ Electrical interface

#### 10GBASE-X

- ▶ PCS and PMA sublayers
  - 8b/10b coding
  - PCS code-groups, utilization of control characters for signalling

- Control code groups
- SKIP sequence
- ▶ PMD 10GBASE-LX4
  - Introduction to transmission on optical fiber
  - Wave Division Multiplexing
- ▶ PMD 10GBASE-CX4
  - Using a twinaxial cable
  - Test fixture characteristics

## 10GBASE-W/R PCS

- ▶ 10GBASE-W/R PCS layer
  - Block formats
  - 64b-66b encoder
  - Scrambler
  - Test pattern functionality
- ▶ WAN Interface Sublayer (10GBASE-W)
  - Introduction to SONET / SDH
  - Framing, scrambling, defect/anomaly detection
  - Mapping of data-units from the PCS into the payload capacity of a STS-192c SPE
  - Receiver, delineation of octet boundaries, checking the BIP octets
  - Error propagation
- ▶ PMA type serial
  - XSBI interface
  - Signal detect handling
- ▶ PMD, TYPE 10GBASE-S, 10GBASE-L, 10GBASE-E
  - Link power budgets
  - Tests
  - PMD registers
- ▶ APM QT2035 SFI/XFI-XAUI PHY and S19235 SONET/SDH transceiver

## ELECTRICAL DISPERSION COMPENSATION

- ▶ Chromatic dispersion
- ▶ Polarization dispersion
- ▶ Modal dispersion
- ▶ Equalization algorithms
- ▶ Linear vs Limiting electrical interface

## PMD, TYPE 10GBASE-LRM (Long Reach Multimode)

- ▶ Preferred launch, alternative launch
- ▶ Fiber types
- ▶ Measurement methods

## 10GBASE-T

- ▶ 16-level PAM signaling
- ▶ Two-dimensional (2D) symbols
- ▶ 2D symbol selection from a constrained constellation of 128 maximally spaced 2D symbols
- ▶ 65-bit block formats
- ▶ Link training, master / slave operation
- ▶ Scrambling
- ▶ Signaling, forward error correction
- ▶ Test pattern generators
- ▶ PMA stages
- ▶ Compensating for signal attenuation
- ▶ 10GBASE-T PHY specific registers

- ▶ Auto-negotiation, page utilization
- ▶ MDI specification, automatic MDI/MDI-X configuration
- ▶ Test modes, test fixtures

### **ENHANCED SMALL FORM FACTOR PLUGGABLE MODULE SFP+**

- ▶ Low speed electrical and power specification
- ▶ High speed electrical specification
- ▶ I2C interface

### **10G BACKPLANES**

- ▶ Introduction to 10G backplane clauses
- ▶ 10GBASE-KX4
- ▶ 10GBASE-KR
- ▶ Autonegotiation for Ethernet backplanes
- ▶ Forward Error Correction (FEC)

## **Renseignements pratiques**

**Duration : 3 days**  
**Cost : 2390 € HT**