This course covers the software and hardware implementation of ST Spear 1310 high-end SoC

Objectives

- The course details the hardware implementation of the SPEAr1310 SoC.
- The course focuses on the boot sequence, the clocking and the power management strategies.
- The course explains all parameters that affect the performance of the system in order to easily perform the final tuning.
- The interfaces to high speed bus, such as PCIe, SATA and Ethernet are covered in depth.
- An overview of the Cortex-A9MP core helps to understand issues caused by MMU, cache and snooping.
- Interrupt management through ARM GIC is explained through a lab.
- The course also covers the hardware implementation, particularly the DDR3 and NAND flash controllers.

- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-A9 core. Our course reference RA2 - Cortex-A9 implementation course details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - CAN bus, reference IA1 - CAN buscourse
  - SD / MMC, reference IS2 - eMMC 5.0course
  - SATA, reference IS3 - Serial ATA IIIcourse
  - PCI, reference IC1 - PCI 3.0course
  - PCI Express, reference IC4 - PCI Express 3.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

DAY 1

ARCHITECTURE OF SPEAr1310

- ARM core based architecture
- On-chip memories
- Clarifying the internal data paths: AXI interconnect, NOC, peripheral buses
- Organization of a board based on SPEAr1310
- Memory mapping

THE ARM CORTEX-A9MP CORE - OVERVIEW

- Presentation of the core, architecture and programming model
- MMU and TLBs
- Level 1 caches
- Cache coherency
- Level 2 cache
- Timers and watchdogs
- Parity protection

DAY 2

POWER CONTROL MODULE, RESET AND CLOCK GENERATOR (RCG)

- PCM
- Generation of supply switch control signals for power islands
- Generation of shutoff commands for external DDR 1V2 and 1V5/1V8 supply lines
- Monitoring of voltage detector outputs for each power island
- Selecting wake-up sources
- Clock Manager
- Clock sources
- Integrated PLLs
- Clock generators
- System Reset Controller
- System boot mode selection
- Hardware initialization phase
- Startup sequence

SYSTEM CONTROL

- IOMUX module

- General Purpose Input interrupt request capability
- Keyboard controller
- Integrated semaphores
- Temperature sensor

THE CORTEX-A9MP PLATFORM

- Cortex-A9MP and PL310 L2 cache IP instantiation options
- Integrated interrupt controller (GIC), detail of interrupt mapping
- Implementing hardware coherency between IO masters and cluster through ACP
- Multi-layer interconnect matrix, crossbars and shared link
- Connectivity matrix

CORTEX-A9 CORESIGHT SUBSYSTEM (A9CS)

- Introduction to CoreSight, DAP features
- Program Trace Macrocell
- Cross Triggering Interfaces

DAY 3

GENERAL PURPOSE PERIPHERALS

- Timers
- 4x General-Purpose Timer and High Resolution Timer
- Real Time Clock
- DMA controllers
- DMA multiplexer
- Multi-block transfers achieved through linked lists
- Programmable channel priority
- 16 handshaking interfaces for source and destination peripherals
- Analog-to-Digital converter
- 10-bit resolution
- 8 analog input channels
- DMA hardware handshaking interface

MASS-STORAGE INTERFACES

- Serial Management Interface
- SATA II
- Controlling the state of the 3 SATA ports
- Initialization of the controller
- AHCI software host Interface
- Hardware-assisted native command queuing for up to 32 entries
- Integrated DMA channels
- Memory Card Interface (MCIF)
- SD, MMC and SDIO protocols support
- Compact Flash/CF+ Host controller

DAY 4

ACCESSING EXTERNAL MEMORY-MAPPED RESOURCES

- Multi-Port DDR Controller
- Introduction to DDR2 and DDR3, write-leveling, ZQ calibration
- Pinout, clocking
- DDR calibration and delay-lines
- Advanced bank look-ahead features for high memory throughput

- Setting DDR-device specific timing parameters
- Reporting errors
- Flexible Static Memory Controller
- External device address mapping
- Interfaces with static memory-mapped devices including NOR flash, SRAM, Cellular SRAM and CosmoRAM
- NAND flash controller with hardware ECC
- External asynchronous wait control
- PCI controller
- 32-bit / 66-MHz operation
- Programmable for acting as host or device
- PCI Express controller
- Muxing SATA and PCIe onto high-speed lanes
- Configuration as Agent or Root Complex
- Interrupt management
- Hot plug support
- Error management

DAY 5

COMMUNICATION CONTROLLERS

- Synchronous Serial Port
- I2C interfaces
- UART
- USB
- Integrated USB2.0 PHYs
- Explaining what is OTG, SRP and HNP
- High-speed operation
- EHCI support, muxing periodic and non-periodic traffics
- Full speed operation, OHCI
- Gigabit Ethernet Controller
- PHY connection
- Incoming frame filtering mechanisms, hash tables
- VLAN support
- TCP-IP offload
- Audio video (AV) feature, transmitting time-sensitive informations
- IEEE1588 protocol support, timestamp registers
- Media Information Base
- CAN controller
- CAN protocol basics
- message objects

SECURITY

- One Time Programming interfaces
- Security Coprocessor C3
- Multipurpose, instruction driven, programmable DMA-based co-processor
- Sequence to encrypt / decrypt data
- Sequence to generate / check a SHA signature

Renseignements pratiques

Inquiry : 5 days