STR3 - STR91X implementation

This course covers STR9 ARM-based MCU family

Objectives

- The course details the hardware implementation of the STR91x microcontrollers.
- The boot sequence and the clocking are explained.
- The course focuses on the low level programming of the ARM966 CPU.
- Practical labs on integrated peripherals are based on I/O functions provided by ST.

- Note that ACSYS does not sell emulation probes and IDEs. Consequently this course has not been designed to convince attendees to buy a particular IDE. The unique objective consists in providing sufficient knowledge to attendees so that they can successfully design a system based on STR9.

- This course has been delivered several times to companies developing embedded systems, such as industrial equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence, the vector table and the operation of embedded peripherals.

- *They have been developed with 2 different IDEs : Keil and IAR.*
- *Consequently for on site course, it is up to the customer to select the IDE under which labs will be run.*

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- This course provides an overview of the ARM966 core. Our course reference R1 - ARM7/9 implementationcourse details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented

- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO STR91XF

Overview

- ARM core based architecture
- Features of AHB and APB buses
- The main three blocks : platform, core and input / output peripherals

THE PROCESSOR CORE

THE ARM966E-S CPU

- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- Pipeline, calculation of the CPI
- Branch cache
- Clarifying the data path
- Tightly Coupled Memories
- ARM vs Thumb instruction sets, interworking
- Stack management
- Benefits of condition set capability in ARM state
- C-to-Assembly interface
- Exception mechanism, handler table
- Debug facilities

PLATFORM

INFRASTRUCTURE

- AHB/APB Bridges, split transactions, error handling
- Internal 96 KB SRAM,
- Flash memory
- Program and erase sequences
- VIC Interrupt controller
- Wake-up / interrupt unit
- System timers : Real Time Clock, Watchdog timer

HARDWARE IMPLEMENTATION

- Low voltage detectors
- Clocking
- Reset causes
- Start-up sequence, fetch of the first instruction
- Low power modes
- External Memory Interface
- I/O Ports

INTEGRATED I/Os

NON COMMUNICATION ORIENTED INPUT / OUTPUT PERIPHERALS

- Timers
  - Output compare and input capture capabilities, force compare modes
  - One pulse mode
  - Output PWM mode, on-the-fly modification of the duty cycle
  - Input PWM mode, pulse measurement
- DMA controller
  - Request priority management between the 16 channels
  - Scatter / gather operation, transfer descriptor chaining
  - Error management
- Analog-to-Digital Converter
  - One-shot or continuous conversion
  - Analog watchdog with interrupt generation
- 3-phase induction motor controller
  - Tacho counter operating modes
  - Rotor speed measurement
  - Dead time generator

COMMUNICATION CONTROLLERS

- I2C interface
  - I2C protocol basics
  - Slave mode vs master mode
  - Support for DMA
- Synchronous Serial Peripheral [SSP]
  - SPI protocol basics
  - Queue mode operation
  - Transfer sequence
- UART
  - Queue operation mode
  - Hardware flow control
  - IrDA mode
  - Support for DMA
- CAN controller
  - CAN protocol basics
  - CAN controller organization
  - Message objects
  - Filtering of received messages
  - FIFO mode management
- USB slave interface
  - USB protocol basics
  - Buffer description block, buffer descriptor table
  - DMA controller used to move data between buffers and EndPoints
  - Endpoint initialization
- Fast Ethernet controller
  - 802.3 MAC basics
  - Connection to the PHY : MII bus
  - Management interface, auto-negotiation
  - DMA controller operation
  - Frame filtering
  - VLAN support
  - Error management

Renseignements pratiques

Duration : 4 days
Cost : 1500 € HT