TI2

This course covers all MCUs belonging to the Stellaris Cortex-M4F family, LM4F100 and LM4F200 SERIES.

Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M4F core architecture
  - Becoming familiar with CCS or Keil IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and the implementation of the TI Driver Lib.
- Note that this course has been designed from the architecture of the most complex STELLARIS Cortex-M4 based device, the LM4F232.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.

- ACSYS is able to assist the customer by providing consultancies
  - Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS porting and uIP /LWIP or Interniche stack integration.

- According to the actual reference chosen by the customer, some chapters may be removed

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M4F core. Our course reference RM3 - Cortex-M4 / Cortex-M4F implementation course details the operation of this core and particularly details the operation of FPU and DSP instructions.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- **The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.**
- **Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented**
- **At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.**
  - **In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.**

Plan

ARCHITECTURE OF STELLARIS MCUs

- ARM core based architecture
- Description of Series LM4F100 and LM4F200 SoC architecture
- Clarifying the internal data and instruction paths
- Highlighting possible concurrent transactions
- Integrated memories
- SoC mapping

THE ARM CORTEX-M4F CORE

- V7-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism
- Memory Protection Unit
- Floating Point unit and DSP instructions

BECOMING FAMILIAR WITH CODE COMPOSER STUDIO OR KEIL IDE

- Getting started with the IDE
- Parameterizing the compiler / linker
- Creating a project from scratch
- C start program

PROGRAMMING AND DEBUGGING

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Integrated ARM Serial Wire Debug

RESET, POWER AND CLOCKING

- Reset
- Clocking
- Power control

INTERNAL INTERCONNECT

- Bus matrix
- µDMA

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module

INTEGRATED MEMORIES

- Flash memory, this module is not implemented in all STELLARIS devices
- Internal SRAM
- Internal ROM
- Internal EEPROM

TIMERS

- General Purpose Timer Module block
- Capture Compare PWM pins
- Watchdog timers
- Advanced Motion Control

ANALOG MODULES

- 10-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- Analog comparators

CONNECTIVITY AND COMMUNICATION

- SSI
- UART
- I2C
- CAN
- USB Host, Device and OTG

Renseignements pratiques

Duration : 5 days
Cost : 1950 € HT