



AT3 - AT91RM9200 microcontroller implementation

This course covers AT91RM9200 ARM-based MCU family

Objectives

- The course details the hardware implementation of the AT91RM9200.
- The ARM920T operation is detailed, particularly cache and MMU.
- The boot sequence and the clocking are explained.
- Practical labs on integrated peripherals are based on I/O functions provided by Atmel.
- The course provides examples of internal peripheral software drivers.
- Note that ACSYS does not sell emulation probes and IDEs. Consequently this course has not been designed to convince attendees to buy a particular IDE. The unique objective consists in providing sufficient knowledge to attendees so that they can successfully design a system based on AT91RM9200.
- This course has been delivered several times to companies developing embedded systems, such as medical equipments.
- Note that an additional day on Linux porting onto an AT91RM9200 board may be appended.

A lot of programming examples have been developed by ACSYS to explain the boot sequence, the vector table and the operation of embedded peripherals.

- They have been developed with 2 different IDEs : Keil and IAR.
- Consequently for on site course, it is up to the customer to select the IDE under which labs will be run.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- This course provides an overview of the ARM920T core. Our course reference [R1 - ARM7/9 implementationcourse](#) details the operation of this core.
- The following courses could be of interest:
 - USB Full Speed High Speed and USB On-The-Go, reference [IP2 - USB 2.0course](#)
 - Ethernet and switching, reference [N1 - Ethernet and switchingcourse](#)
 - CAN bus, reference [IA1 - CAN buscourse](#)

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO AT91RM9200

Overview

- ARM core based architecture, AMBA buses
- The main three blocks : platform, core and input / output peripherals

THE PROCESSOR CORE

THE ARM920T CORE

- Presentation of the core, architecture and programming model
- Operating modes : user, system, super, IRQ, FIQ, undef and abort
- ARM vs Thumb instruction sets, interworking
- Access to memory-mapped locations, addressing modes
- Stack management
- C-to-Assembly interface
- Exception mechanism, handler table
- MMU, format of page descriptor tables
- Cache operation
- Debug facilities

PLATFORM

INFRASTRUCTURE

- Power supplies, internal regulator
- Power-on sequence
- Clock generator, on-chip oscillator, PLL
- Boot program
- Memory controller
- Internal high-speed flash
- External Bus Interface
- Power management controller
- Advanced interrupt controller
- Parallel input / output controller
- Peripheral DMA controller

INTEGRATED I/Os

TIMERS

- Periodic Interval Timer
- Windowed Watchdog
- Real-time timer
- 3-channel timer / counter

COMMUNICATION CONTROLLERS

- 2-wire interface
 - I2C protocol basics

- Transmit and receive sequences
- SPI
 - Master / slave operation
 - External chip-select
 - Transfer sequence
- USART
 - Individual baud rate generators
 - IrDA modulation / demodulation
 - RS485 support
 - Flow control
- Synchronous Serial Controller
 - I2S analog interface support
 - Time Division Multiplexed support
 - High speed continuous data stream capabilities
- Ethernet MAC
 - Full duplex vs half duplex operation
 - Accessing PHY registers, auto-negotiation
 - Receive and Transmit buffer management, buffer descriptors
 - Incoming frame filtering
- USB device
 - Full speed operation
 - Endpoint configuration
- USB host
 - Overview of the OHCI specification
 - Understanding how USB packets are prepared and scheduled for transmission, transfer descriptor
- Multimedia Card Interface (on demand)
 - MMC and SD card basics
 - Command / response protocol
 - Read sequence
 - Write sequence
 - Related interrupts