AT4 - AT91SAM3 series implementation

This course covers AT91SAM3S, AT91SAM3U and AT91SAM3N ARM-based MCU family

Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M3 core architecture
  - Becoming familiar with the IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex AT91SAM3 device, the AT91SAM3S4C.
- Consequently, a chapter has been designed by Acsys for each possible integrated IP.
  - According to the actual reference chosen by the customer, some chapters may be removed.
- Products and services offered by ACSYS:
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS porting and uIP /LWIP stack or Interniche stack integration.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the ARM Cortex-M3 core. Our course reference RM2 - Cortex-M3 implementation course details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - SD / MMC, reference IS2 - eMMC 5.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

ARCHITECTURE OF AT91SAM3 MCUs

- ARM core based architecture
- Description of AT91SAM3N, AT91SAM3U and AT91SAM3S SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AHB-to-APB bridge
- Integrated memories
- SoC mapping

THE ARM CORTEX-M3 CORE

- V7-M core family
- Core architecture
- Programming
- Exception behavior, exception return
- Basic interrupt operation, micro-coded interrupt mechanism
- Memory Protection Unit

BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 IDEs: Keil, IAR and GCC / Lauterbach.
- Thus the customer has just to indicate which one he has chosen.
- Getting started with the IDE
- Parameterizing the compiler / linker
- Creating a project from scratch
- C start program

PROGRAMMING AND DEBUGGING

- Debug architecture
- Programming

RESET, POWER AND CLOCKING

- Power control
- Reset controller
- Clocking
- Low power modes

INTERNAL INTERCONNECT

- Bus matrix
- Peripheral DMA Controller (PDC)
- DMA Controller (DMAC), AT91SAM3U

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module

INTEGRATED MEMORIES

- Embedded flash memory

- Internal SRAM
- Internal ROM

MEMORY INTERFACE

- High Speed MultiMedia Card Interface
- Static Memory Controller

TIMERS

- Timer counter
- PWM
- Real-time Timer
- Real-time Clock
- Watchdog timer

ANALOG MODULES

- 12-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- 12-bit Analog-to-Digital Converter, ADC12B, AT91SAM3U
- 12-bit Digital-to-Analog Converter
- Analog Comparator Controller

SECURITY AND INTEGRITY

- Cyclic Redundancy Check Calculation Unit
- Chip Identifier

CONNECTIVITY AND COMMUNICATION

- SPI
- Synchronous Serial Controller
- UART
- USART
- Two-Wire Interface
- USB Device FS
- USB Device HS, AT91SAM3U
- ISO7816 smartcard interface