This 2-day course covers the eMMC 5.0 specification

Objectives

- This course explains the Command – Data – Response protocol.
- The hardware layer is detailed, including the analog part.
- The course clarifies the compatibility between SD and MMC/eMMC specifications.
- The course describes the low power modes.
- Secure aspects, such as secure erase and authenticated transfers are explained.
- An example of eMMC host controller is studied.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge of a bus protocol is recommended

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

OVERVIEW

- Objectives of MMC/eMMC specification, relationship with SD
- High capacity devices
- Speed class definition
- Mechanical standards

PHYSICAL LAYER

- Pinout
- Power Saving Sleep mode
- Reset sources
- Power cycling
- Bus speed modes
- Single ended signaling with 4 drive strengths
- Signaling levels of 1.8V and 1.2V
- Tuning concept for read operations
- HS200 adjustable sampling host
- Bidirectional strobe in HS400

INITIALIZATION SEQUENCE

- Device reset to Pre-idle state
- Information registers
- Session address
- Boot area partitions
- Device identification process
- Power class selection
- Power class selection
- Accesses to the Replay Protected Memory Block

BUS PROTOCOLS

- Command – Response – Data block structure tokens
- Multiple-block read and write operations
- CRC status
- Timings
- Bus modes overview
- Error conditions

SECURITY

- • Secure mode, secure removal
- Write protect management
- Production state awareness
- Replay Protected Memory Block, authenticated data transfers
- Security protocol commands
- Field firmware update
- Device lock/unlock operation

eMMC FUNCTIONAL DESCRIPTION

- High priority interrupt (HPI)
- Background Operations
- Real Time Clock
- Partition attributes
- Context management
- System data tagging
- Packed commands
- Dynamic device capacity
- Optional volatile cache
- Boot areas that will automatically stream data when using defined boot modes
- Context writing interruption

HOST CONTROLLER INTERFACE

- Example of NXP uSDHC

- Managing initialization
- Relying on DMA to transfer data blocks

Renseignements pratiques

Inquiry : 2 days