FC1 - MPC755 implementation

This course covers NXP G3 Power CPU

Objectives

- The training aims to understand the PowerPC programming environment through the MPC755 processor.
- A focus is done on the PowerPC EABI which is fundamental when C programs are to be interfaced with assembly routines.
- The pipeline is viewed in detail in order to infer instructions scheduling guidelines.
- Many Diab Data PowerPC specific compiler options are studied.
- A flush routine is used to clarify the data path between L1 data cache, L2 cache and SDRAM main memory.
- The course details the segmentation / pagination mechanism used to protect process.
- A generic exception handler is described.
- The hardware implementation and particularly the analysis of the L2 bus timings are handled with great care.
- This course has been delivered several times to companies involved in the design of avionics critical systems.

A more detailed course description is available on request at training@ac6-training.com

Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

THE INSTRUCTION PIPELINE

- MPC755 implementation : superscalar operation, out-of-order execution, register renaming, serializations, isync instruction.

- Branch processing unit : BTIC, static prediction vs dynamic prediction, speculative loads, guarded memory.
- Branch instructions.
- Coding guidelines.

DATA AND INSTRUCTION PATHS

- Load / store buffers
- Sync and eieio instructions
- Store gathering mechanism

CACHES

- Cache basics
- L1 caches: PLRU algorithm
- Shared resource management
- Cache coherency mechanism
- The MEI state machine
- Management of cache enabled pages shared with PCI DMAs
- Reservation coherency, management of Boolean semaphores in a multi-processor system
- Cache related instructions
- Cache flush routine
- The L2 cache, organization, replacement algorithm
- Implementation of a private memory

SOFTWARE IMPLEMENTATION

- PowerPC architecture specification, the 3 books UISA, VEA and OEA
- 7XX registers
- addressing modes
- Integer instructions
- IEEE754 basics
- Floating point load / store instructions
- Floating point arithmetical instructions
- The PowerPC EABI
- Linking an application with Diab Data

THE MMU

- Thread vs process
- Introduction to real, block and segmentation / pagination translations
- Memory attributes and access rights definition
- Virtual space benefit, page protection through segmentation
- TLBs organization
- Segmentation : process ID definition
- Pagination : PTE table organization, tablesearch algorithm
- Benefits of the software tablewalk in comparison with the hardware tablewalk
- MMU implementation in real-time sensitive applications

THE EXCEPTION MECHANISM

- Save / restore registers SRR0/SRR1, rfi instruction
- Exception management mechanism
- Registers updating according to the exception cause
- Requirements to allow exception nesting

HARDWARE IMPLEMENTATION

- Hreset vs Sreset
- Bus operation
- Address phase
- Data phase

- Address decode logic design
- Minimal implementation
- The L2 bus, supported synchronous SRAM technologies
- Objectives of the DLL
- Timing analysis, AN1794/D
- Low power modes
- Discrete signals

THE PERFORMANCE MONITOR

- Objectives of the performance monitor
- Event counting
- Programming interface

THE DEBUG PORT

- JTAG emulation
- Real time trace requirements
- Code instrumentation
- Hardware breakpoints

Renseignements pratiques

Inquiry : 5 days