[redacted]

This course describes the PTP protocol and provides implementation examples

Objectives

- The course explains the IEEE1588 standard and details some implementation solutions
- The BMC algorithm is described
- The course emphasizes the way to implement IEEE1588 on an Ethernet system and highlights the boundary between software and hardware
- The new features of P1588 (aka IEEE1588v2) are studied

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of Ethernet and switching is needed, see our course reference N1 - Ethernet and switchingcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

Introduction

- Objectives of the standard
- The need for synchronization

- Definitions

PTP Clock Synchronization Model

- The PTP messages
- PTP systems, acyclic graph structure
- Message filtering
- Clock properties, stratum, identifier
- Subdomain properties

PTP Protocol Specification

- Model of a subdomain of PTP clocks
- State behavior of clocks
- Protocol engine state machine
- Clock data sets, initialisation properties
- Messaging and internal event behavior of clocks
- Sync-event time-out mechanism
- Synchronization changes of the local clock
- Best Master Clock algorithm
- Clock variance computation
- Local clock synchronization
- Physical requirements for PTP implementations
- Management messages

Ethernet Implementation of PTP

- Ethernet frame type
- IP header and multicast addresses
- UDP header, assigned port numbers
- UDP payload, organization of PTP messages

NXP Implementation of PTP

- eTSEC Ethernet MAC
- Time-stamping
- Clock correction
- Trigger inputs
- Alarms

P1588 aka PTPv2

- Mapping to DeviceNet and Ethernet layer-2
- Prevention of error accumulation in cascaded topologies
- Rapid network reconfiguration
- Extensions to enable implementation of redundant systems
- Optional shorter frame

Renseignements pratiques

Inquiry : 1 day