STR16 - STM32L0

This course descirbe the STM32L0 architecture and practical examples

Objectives

- Understand the Cortex-M0+ core and the STM32L0 SoC.
- Configure RCC (MSI/HSI16/HSE/LSI/LSE), PLL, and prescalers correctly.
- Use GPIO/EXTI, timers/LPTIM, DMA, ADC/COMP, and serial buses.
- Apply ultra-low-power modes and measure consumption.
- Manage Flash, true Data EEPROM (on L0), Option Bytes, and watchdogs.
- (If present) bring up USB FS device and TSC capacitive touch.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:
  - For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.
  - Quizzes are offered at the end of sections that do not include practical exercises to verifythat the trainees have assimilated the points presented

- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

Day 1

Cortex-M0+ overview (core)

- Core overview
- Programmer's model
- Exceptions, NVIC priorities.
- SysTick, SVC, PendSV basics.
- Faults on v6-M → HardFault.
- WFI/WFE sleep entry.
- SWD; optional SWO/ITM.

Exercise: *Exception Management*

SoC & memory map

- Lines (L0x1/L0x2/L0x3).
- Flash / SRAM / PPB map.
- Peripheral address zones.
- UID and Flash size regs.
- Option Bytes overview.

Exercise: *Map & IDs*

RCC - reset & clocks (ULP focus)

- MSI ranges (low-freq steps).
- HSI16 / HSE basics.
- PLLs (device-dep.).
- SYSCLK mux; AHB/APB divs.
- CCIPR.
- MCO output; CSS/HSECSS.

Exercise: *Clock profiles*

Power & voltage scaling

- Sleep / Low-power run.
- Low-power sleep / Stop.
- Standby / VBAT domain.
- Voltage scaling (Range x).
- PVD/BOR levels (OB).
- Fast wake-up notes.

Exercise: *Mode sweep*

GPIO / EXTI / SYSCFG

- PP/OD, pulls, speeds.
- AF mapping rules.
- EXTI lines & priorities.
- Debounce strategies.
- Safe I/O at reset.

Exercise: *GPIO & EXTI*

Timers & LPTIM

- PWM edge/center.
- Input capture basics.
- One-pulse mode.
- Encoder interface.
- LPTIM periodic wake.

Exercise: *PWM + capture*

Day 2

DMA

- Channels/requests map.
- Normal vs circular.
- HT/TC/TE IRQ flags.
- Throughput vs latency.

Exercise: *UART RX ring*

ADC & analog (COMP)

- 12-bit ADC basics.
- Sampling time, ranks.
- Timer-triggered ADC.
- DMA continuous/circular.
- Analog watchdog.
- COMP to EXTI/timers.

Exercise: *ADC + DMA stream*

RTC & tickless timing

- LSE vs LSI trade-offs.
- Calendar, alarm, wakeup.
- Backup registers (VBAT).
- Tickless via RTC/LPTIM.

Exercise: *Tickless blink*

USART / LPUART

- 8/9-bit, parity/stop.
- Oversampling 16/8.
- Blocking / IRQ / DMA.
- LPUART Stop-mode wake.
- Error recovery (ORE/FE).

Exercise: *DMA UART*
Exercise: *LPUART wake from Stop*

SPI

- CPOL/CPHA modes.
- Data sizes; NSS rules.
- Full-duplex DMA.
- Simplex options.
- Timing check (LA).

Exercise: *SPI loopback DMA*

I²C

- Sm/Fm/Fm+ speeds.
- 7/10-bit addressing.
- Analog/digital filters.
- Timeouts; bus-clear.
- Clock stretching.

Day 3

USB FS device (L0x2 variants)

- VBUS sense options.
- EP/FIFO sizing basics.
- CDC/DFU quick paths.
- Clocking constraints.
- Suspend/resume flow.

Exercise: *CDC echo or DFU*

TSC capacitive touch (variants)

- Channel groups/IOs.
- Acquisition timing.
- Threshold setting.
- Noise filtering tips.
- Simple slider/key.

Exercise: *Touch key demo*

Flash, Data EEPROM & OB

- Flash erase/program.
- True Data EEPROM use.
- Simple wear leveling.
- OB: RDP/PCROP/BOR.
- Read reset cause regs.

Boot, ROM & watchdogs

- ROM bootloader ports.
- DFU/UART/I²C options.
- Boot pins & OB links.
- IWDG vs WWDG basics.
- Reset cause logging.

Exercise: *IWDG + DFU try*

Production checklist (wrap-up)

- Clocking proven (MCO).
- I/O safe at boot/sleep.
- Low-power numbers noted.
- Comms error policy set.
- UID/serial/CRC scheme.

Exercise: *Self-audit*

Renseignements pratiques

Inquiry : 3 days