STR18 - STM32 L4/L4+ implementation

This course describe the STM32 L4/L4+ architecture and practical examples

Objectives

- Understand the Cortex-M4F core, DSP/FPU, and the L4/L4+ SoC.
- Configure RCC (MSI/HSI16/HSE/LSI/LSE) and PLL; validate prescalers.
- Use GPIO/EXTI, timers/LPTIM/RTC, DMA/DMAMUX, ADC/COMP/OPAMP/DAC.
- Apply ultra-low-power modes; measure current and wake latency.
- Bring up USART/SPI/I²C/SAI/DFSDM (where available).
- Use SDMMC + FatFS, QSPI/OSPI (variant), USB FS device.
- Manage Flash, Option Bytes, watchdogs, reset causes, and production checklists.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- Practical activities
  - Practical activities represent from 40% to 50% of course duration.
  - Code examples, exercises and solutions
  - For remote trainings:
    - One Online Linux PC per trainee for the practical activities.
    - The trainer has access to trainees' Online PCs for technical and pedagogical assistance.
    - QEMU Emulated board or physical board connected to the online PC (depending on the course).
    - Some Labs may be completed between sessions and are checked by the trainer on the next session.
  - For face-to-face trainings:
    - One PC (Linux ou Windows) for the practical activities with, if appropriate, a target board.
    - One PC for two trainees when there are more than 6 trainees.
  - For onsite trainings:
    - An installation and test manual is provided to allow preinstallation of the needed software.
    - The trainer come with target boards if needed during the practical activities (and bring them back at the end of the course).
- Downloadable preconfigured virtual machine for post-course practical activities
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed in two different ways, depending on the course:
  - For courses lending themselves to practical exercises, the results of the exercises are checked by the trainer while, if necessary, helping trainees to carry them out by providing additional details.

- Quizzes are offered at the end of sections that do not include practical exercises to verifythat the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

Day 1

Cortex-M4F overview (core)

- Programmer's Model
- Exceptions and NVIC priorities.
- DSP intrinsics (SIMD/MACC).
- FPU (single-precision).
- WFI/WFE sleep entry.
- ITM/SWO printf (if present).

Exercise: *Exception Model*
Exercise: *Privilege Mode and Stack*

L4/L4+ SoC & memory map

- AHB/APB buses and bridges.
- Flash/SRAM/CCM (if any) layout.
- Peripheral address map.
- UID & Flash-size registers.
- Option Bytes snapshot.

Exercise: *Map & IDs*

RCC - reset & clocks

- MSI ranges and auto-cal.
- HSI16 / HSE basics.
- PLLs.
- SYSCLK mux; AHB/APB divs.
- CCIPR kernel clocks.
- MCO output; CSS.

Exercise: *Clock profiles*

Power & voltage scaling

- Voltage scaling VOS ranges.
- Low-power run/sleep.
- Stop / Standby modes.
- VBAT/backup domain.
- PVD/BOR levels.

Exercise: *Mode sweep*

GPIO / EXTI / SYSCFG

- PP/OD, pulls, speed/drive.
- AF mapping principles.
- EXTI lines & priorities.
- Safe I/O at reset.

Exercise: *EXTI + GPIO*

Timers & LPTIM

- PWM edge/center.
- Input capture, one-pulse.
- Encoder interface.
- Master/slave triggers.
- LPTIM for tickless.

Exercise: *PWM + capture*

Day 2

DMA / DMAMUX

- DMA1/DMA2 overview.
- Requests via DMAMUX.
- Normal vs circular.
- HT/TC/TE events.
- Restart & error paths.

Exercise: *UART RX ring (DMA)*

ADC & triggers

- Resolution & sampling time.
- Oversampling & alignment.
- Timer-triggered regular.
- Injected group basics.
- DMA circular streaming.
- Analog watchdog.

Exercise: *ADC + DMA stream*

OPAMP / COMP / DAC

- OPAMP PGA modes.
- COMP thresholds/hysteresis.
- Routing to timers/EXTI.
- DAC 12-bit with S&H.
- Calibrate & verify.

Exercise: *Analog chain*

USART / LPUART

- USART/LPUART Overview.
- Oversampling 16/8.
- Blocking/IRQ/DMA.
- LPUART Stop-wake.
- Error handling (ORE/FE).

Exercise: *Robust UART*
Exercise: *LPUART wake from stop*

SPI / I²S / SAI (variant)

- SPI CPOL/CPHA, NSS.
- Data sizes & duplex.
- DMA transfers.
- I²S basic audio path.
- SAI TX/RX blocks.

Exercise: *SPI loopback DMA*

I²C

- Sm/Fm/Fm+ speeds.
- 7/10-bit addressing.
- Analog/digital filters.
- Timeouts; bus-clear.
- Clock stretching.

Day 3

RTC & tickless timing

- LSE vs LSI trade-offs.
- Calendar, alarm, wakeup.
- Backup registers.
- Tickless via RTC/LPTIM.
- Drift/calibration.

Exercise: *Tickless blink*

USB FS device (variant)

- VBUS sense options.
- EP/FIFO sizing basics.
- CDC/DFU quick paths.
- Clocking constraints.
- Suspend/resume flow.

Exercise: *CDC echo or DFU*

Audio front-end (variant: DFSDM/SAI)

- DFSDM filter paths.
- Oversampling & decimation.
- SPI/I²S microphones.
- DMA to circular buffer.
- Basic RMS meter.

Exercise: *DFSDM stream*

Storage & external memory

- SDMMC + FatFS basics.
- QSPI mapped mode.
- OSPI (L4+ variants).
- Buffer align/invalidate.
- File-I/O sanity tests.

Exercise: *SD + FatFS*

Day 4

Low-power measurement

- GPIO leakage strategy.
- Kernel clocks for LP.
- Stop entry/exit timing.
- DMA + LP coexistence.
- Practical power tips.

Exercise: *Measure Sleep/Stop*

Security & integrity (variant)

- RNG TRNG.
- AES/HASH engines.
- PKA (L4R/L4S).
- CRC for images/packets.
- Key storage basics.

Exercise: *CRC/AES*

Flash, OB & robustness

- Flash erase/program.
- EEPROM emulation.
- OB: RDP/PCROP/BOR.
- Watchdogs IWDG/WWDG.
- Reset cause logging.

Boot, ROM & production checklist

- ROM bootloader ports.
- DFU/UART/I²C options.
- Boot pins & OB ties.
- Version/UID/CRC tags.
- Final audit list.

Exercise: *Self-audit*

Renseignements pratiques

Inquiry : 4 days