FCQ2 - P2020 QorIQ implementation

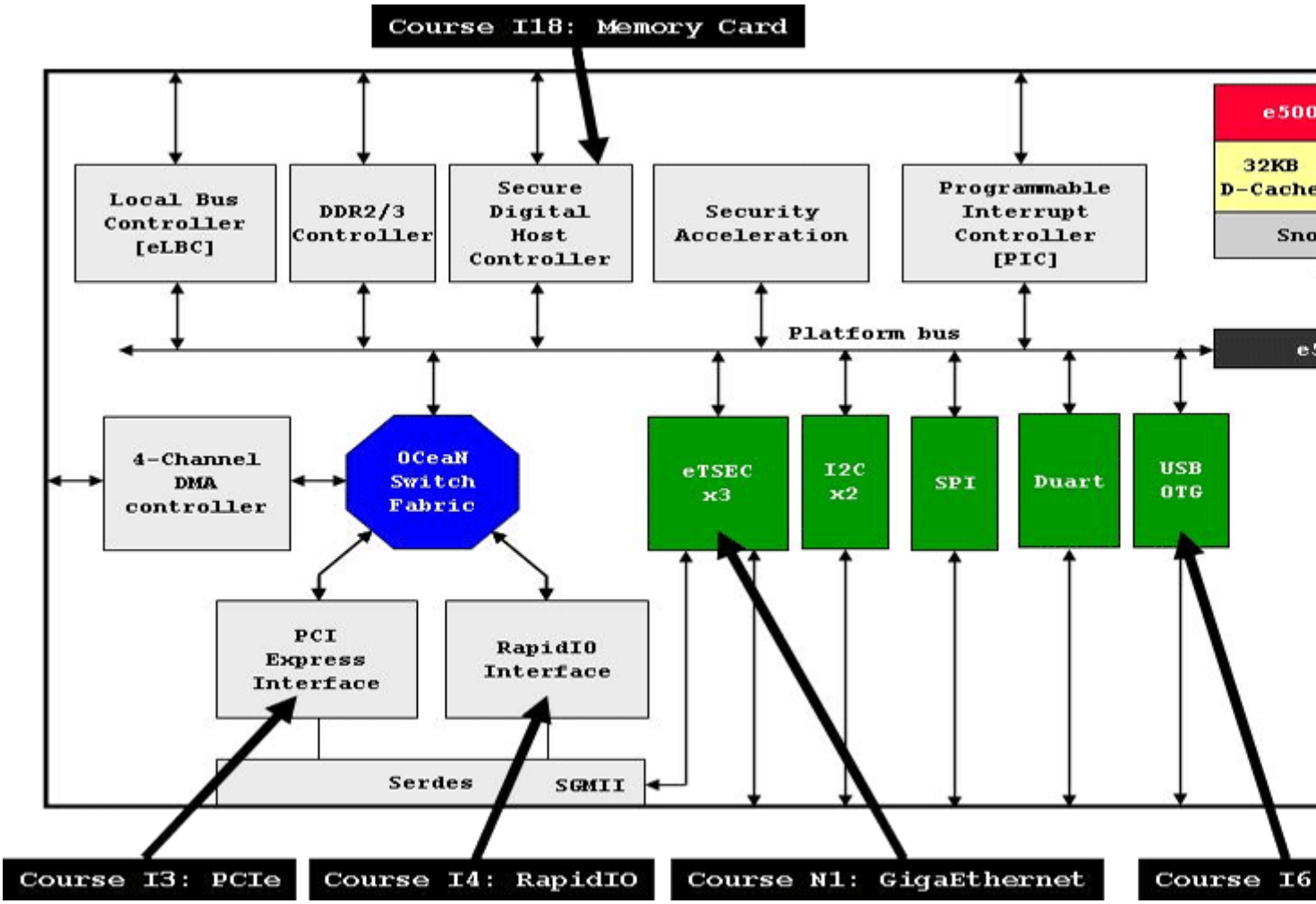
This course covers NXP QorIQ P2010 and P2020

Objectives

- The course clarifies the architecture of the P20X0, particularly the operation of the coherency module that interconnects the e500s to memory and high-speed interfaces.
- Cache coherency protocol is introduced in increasing depth.
- The e500 core is viewed in detail, especially the SPE unit that enable vector processing.
- The boot sequence and the clocking are explained.
- The course focuses on the hardware implementation of the P20X0.
- A long introduction to DDR SDRAM operation is done before studying the DDR2/3 SDRAM controller.
- An in-depth description of the RapidIO port and the PCI-Express port is done.
- The course explains how to implement QoS on GigaEthernet controllers.

- ACSYS has developed an optimized SPE based FFT coded in assembler language.
- Performance for 1024 complex floating point single precision samples is:
  - - 91_386 core clock cycles without reverse ordering, 94_124 with reverse ordering
- Performance for 4096 complex floating point single precision samples is:
  - - 470_778 core clock cycles without reverse ordering, 511_227 with reverse ordering
- For any information contact training@ac6-training.com

Related courses



Prerequisites

- Experience of a 32-bit processor or DSP is mandatory.
- Knowledge of RapidIO and PCI Express is recommended.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO P20X0

Overall description

- Internal data flows, OCEAN switch fabric, packet reordering
- Implementation examples
- Address map, ATMU, OCEAN configuration
- Local vs external address spaces, inbound and outbound address decoding
- Accessing memory-mapped registers from external master

THE e500 CORES

THE INSTRUCTION PIPELINE

- Dual-issue superscalar control, out-of-order execution
- Execution units : 2 simple Integer Units + 1 Complex Integer Unit
- Dynamic branch prediction using a 128-set 4-way set associative Branch Target Buffer
- Execution timing, rename register operation, instruction serialization

DATA AND INSTRUCTION PATHS

- The Core Complex Bus : high speed on-chip local bus with data tagging
- The LMQ, the store queue, the castout queue
- Store miss merging and store gathering
- Memory access ordering
- Lock acquisition and import barriers

THE MEMORY MANAGEMENT UNITS

- The first level MMU and the second level MMU, consistency between L1 and L2 TLBs
- Snooping of TLBs
- TLB software reload, page attributes WIMGE
- Process protection, variable number of PID registers and sharing
- MMU implementation in real-time sensitive applications

CACHES

- The L1 caches, PLRU replacement algorithm, 8-way set associativity, cache block and unlock APU
- Level 2 cache, partition into L2 cache plus SRAM
- Allocation of data transferred by external masters into the cache: stashing
- Snooping mechanism, stashing mechanism
- L2 cache locking

PROGRAMMING

- Differences between the new Book E architecture and the classic PowerPC architecture
- Floating Point units, Double-Precision FP
- Signal Processing APU (SPU) : implementation of the SIMD capability without using a separate unit
- PowerPC EABI : sections, C-to-assembly interface

EXCEPTIONS

- Book E exception handling
- Critical versus non critical
- Handler table
- Exception nesting, recoverability from interrupt
- Core timers : Decrementer, Time Base, Fixed Interval Timer and Software Watchdog

DEBUGGING

- Performance monitoring, counting of events
- JTAG emulation, real time trace when the e500 core executes cached instructions
- Watchpoint logic, triggering capabilities based on user programmable events

INFRASTRUCTURE

RESET, CLOCKING AND INITIALIZATION

- Platform clock
- Voltage configuration selection
- Power-on reset sequence, using the I2C interface to access serial ROM
- Boot page translation
- eSDHC boot
- eSPI boot ROM

e500 COHERENCY MODULE

- I/O arbiter
- CCB arbiter
- Transaction queue
- CCB interface

DDR2/DDR3 SDRAM MEMORY CONTROLLER

- DDR2 and DDR3 Jedec specification
- On-Die termination
- Mode registers initialization, bank selection and precharge
- Command truth table
- Bank activation, read, write and precharge timing diagrams, page mode
- Introduction to the DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Timing parameters programming
- Initialization routine

ENHANCED LOCAL BUS CONTROLLER

- Multiplexed or non-multiplexed address and data buses
- Dynamic bus sizing
- GPCM, UPMs states machines
- Flask Control Machine
- NAND flash controller

SERIAL RapidIO INTERFACE

- Message Unit, direct vs chaining mode operation
- RapidIO doorbell and port-write unit

- Accessing configuration registers via RapidIO packets
- Programming inbound and outbound ATMUs
- Error handling

PCI EXPRESS INTERFACE

- 8-lane PCI Express interface
- Modes of operation, Root Complex / Endpoint
- Transaction ordering rules
- Programming inbound and outbound ATMUs
- Configuration, initialization

PROGRAMMABLE INTERRUPT CONTROLLER

- PIC in multiple-processor implementation
- Interrupt sources : external interrupts, internal interrupts, message interrupts
- Integrated timers
- Interprocessor interrupts
- Per-CPU register usage, message registers
- Nesting implementation

INTEGRATED DMA CONTROLLER

- Priority between the 4 channels
- Support for cascading descriptor chains
- Scatter / gathering
- Selectable hardware enforced coherency

PERFORMANCE MONITOR AND DEBUG FEATURES

- Event counting
- Threshold events
- Chaining, triggering
- Watchpoint facility
- Trace buffer

INPUTS/OUTPUTS

THE ETHERNET CONTROLLERS

- Address recognition, pattern matching
- Buffer descriptors management
- Physical interfaces : GMII, MII, TBI, RGMII, SGMII
- Buffer descriptor management
- Layer 2 acceleration accept or reject on address or pattern match
- 256-entry hash table for unicast and multicast
- Management of VLAN tags and priority, VLAN insertion and deletion
- Quality of service, managing several transmit and receive queues
- TCP/IP offload engine, filer programming
- IEEE1588 compliant time-stamping

ENHANCED SECURE DEVICE HOST CONTROLLER

- Storing and executing commands targeting the external card
- Multi-block transfers
- Moving data by using the dedicated DMA controller
- Dividing large data transfers

- Card insertion and removal detection

USB CONTROLLER

- Dual-role (DR) operation
- EHCI implementation
- ULPI interfaces to the transceiver
- OTG support
- Dedicated DMA channels
- Endpoints configuration

SECURITY ENGINE

- Overview of the encryption mechanism
- Introduction to DES and 3DES algorithms
- Data packet descriptors
- Crypto channels
- XOR acceleration

LOW SPEED PERIPHERALS

- Description of the NS16552 compliant Uarts
- I2C controller
- Enhanced SPI, transmit and receive sequences