FF2 - MCF523X implementation

This course covers MCF523X ColdFire MCUs

Objectives

- The course explains how to write optimized based on pipeline knowledge.
- The memory controller parameterizing is detailed.
- The reset sequence is studied.
- The interrupt controller is viewed in detail.
- The course describes the implementation of the Fast Ethernet controller and the utilization of the cryptography modules.

- This course has been delivered several times to companies developing industrial and transportation equipments.
- Generation of DMA transfers terminated by interrupt

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as Fast Ethernet.
• They have been developed with CodeWarrior compiler and are executed under CodeWarrior debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Related courses

- Ethernet and switching, reference N1 - Ethernet and switchingcourse
- USB 2.0, reference IP2 - USB 2.0course
- CAN bus, reference IA1 - CAN buscourse
- eTPU, reference FM3 - eTPU programmingcourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO MCF523X

Overview

- Coldfire roadmap
- 523X block diagram
- Pinout
- Memory mapped I/O organization

V2E CORE

CORE ARCHITECTURE

- V2E pipeline
- Addressing modes
- Branch, data transfer, arithmetic, logic, shift & rotate, bit instructions
- Mac instructions, implementation of a fixed-point DFT
- C to assembly interface
- Section definition, parameterizing the linker command file
- Exception management
- Internal SRAM
- 523X cache operation
- Power management

DEBUG FACILITIES

- Intrusive vs non-intrusive debug
- BDM port
- Hardware breakpoints
- Trace port

PLATFORM

RESET

- Reset sources
- Clocking
- Reset control flow
- Chip Configuration Module [CCM]
- Requirements of the boot routine

SYSTEM PERIPHERALS

- SCM
- The interrupt controller
- The Edge Port Module
- Watchdog timer module
- Programmable Interrupt Timer Modules

THE DMA CONTROLLER

- Channel prioritization
- Bandwidth control
- Transfer termination
- Utilization of DMA timers

HARDWARE IMPLEMENTATION

- Dynamic bus sizing
- Address decoding
- Data transfer sequence
- Burst cycles

THE MEMORY CONTROLLER AND THE SDRAM CONTROLLER

- The memory controller : SRAM/Flash connection, chip-select programming
- DRAM / SDRAM basics
- The 523X (S)DRAM controller : address decoding, refresh rate definition, address multiplexing selection

INTEGRATED I/Os

COMMUNICATION CONTROLLERS

- The UART Module
- The QSPI
- The I2C controller
- The FlexCAN controller
- The Fast Ethernet Controller

CRYPTOGRAPHY MODULES

- Message Digest Hardware Accelerator
- Random Number Generation
- Symmetric key hardware accelerator, introduction to data encryption standards
- Data flow, management of input and output FIFOs