FK1 - Kinetis MCU Implementation

This course covers all NXP MCUs belonging to the Kinetis families K10, K20, K30, K40 and K60

Objectives

- This course has 5 main objectives:
  - Describing the hardware implementation and highlighting the pitfalls
  - Describing the ARM Cortex-M4 core architecture
  - Becoming familiar with the IDE and low level programming
  - Describing the units which are interconnected to other modules, such as clocking, interrupt controller and DMA controller, because the boot program generally has to modify the setting of these units
  - Describing independent I/O modules and their drivers.
- Note that this course has been designed from the architecture of the most complex Kinetis device, the K60.
  - Consequently, a chapter has been designed by Acsys for each possible integrated IP.
  - So the customer can build its own course outlines from the topics described hereafter.

- Products and services offered by ACSYS:
  - ACSYS has developed FFTs (floating-point and fixed-point) optimized for ARM cores, based on SIMD instructions supported by the Cortex-M4.
  - Contact training@ac6-training.comto obtain informations about the performance of these FFTs.
  - ACSYS is able to assist the customer by providing consultancies. Typical expertises are done during board bringup, hardware schematics review, software debugging, performance tuning.
  - ACSYS has also an expertise in FreeRTOS or MQX porting and uIP /LWIP stack or Interniche stack integration.

This document is necessary to tailor the course to specific customer needs and to define the exact schedule.

Prerequisites and related courses

- This course provides an overview of the Cortex-M4 core. Our course reference RM3 - Cortex-M4 / Cortex-M4F implementation course details the operation of this core.
- The following courses could be of interest:
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - IEEE1588, reference N2 - IEEE1588 - Precise Time Protocolcourse
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

ARCHITECTURE OF KINETIS MCUs

- ARM core based architecture
- Description of K10, K20, K30, K40 and K60 SoC architecture
- Clarifying the internal data and instruction paths: AHB-lite interconnect, peripheral buses, AIPD bridges
- AMBA-to-IPS Re-use IP: ColdFire (AIPS) Controller
- Integrated memories
- SoC mapping

THE ARM CORTEX-M4 CORE

- V7-M core family
- Core architecture
- Freescale on-chip instruction and data cache
- Thumb-2 instruction set
- Exception behavior
- Basic interrupt operation, micro-coded interrupt mechanism
- Memory Protection Unit

V7-M DATA SIGNAL PROCESSING INSTRUCTIONS

- Multiply instructions
- Packing / unpacking instructions
- SIMD packed add/sub instructions
- SIMD combined add/sub instructions
- SIMD multiply and multiply accumulate instructions
- SIMD sum absolute difference instructions
- SIMD select instruction
- Saturation instructions
- Floating point unit
- Cortex Microcontroller Software Interface Standard (CMIS)

BECOMING FAMILIAR WITH THE IDE

- Acsys covers 3 iDEs: CodeWarrior, IAR and GCC / Lauterbach
- Thus the customer has just to indicate which one he has chosen
  - Getting started with the IDE
  - Parameterizing the compiler / linker
  - Creating a project from scratch
  - C start program

PROGRAMMING AND DEBUGGING

- Debug interface
- Programming

RESET, POWER AND CLOCKING

- Reset
- Clocking
- Operation modes

INTERNAL INTERCONNECT

- Crossbar switch
- Hardware Memory Protection Unit
- eDMA

HARDWARE IMPLEMENTATION

- Power pins
- Pinout
- GPIO module

INTEGRATED MEMORIES

- Flex memory, this module is not implemented in all Kinetis devices
- Internal SRAM

MEMORY INTERFACE

- Each Kinetis family supports either a subset or all the following controllers
- FlexBus
- eSDHC
- NAND flash controller
- DRAM controller

TIMERS

- Low Power Oscillator
- COP
- External Watchdog Monitor
- Periodic Interrupt Timer
- Low Power Timer
- Flex Timer
- Carrier Modulator Transmitter

ANALOG MODULES

- 16-bit Analog-to-Digital Converter and Programmable Gain Amplifier
- 12-bit Digital-to-Analog Converter
- Voltage Reference VREF
- High-Speed Comparator HSCMP
- Programmable Delay Block PDB

SECURITY AND INTEGRITY

- Hardware Cyclic Redundancy Check
- Memory-Mapped Cryptographic Acceleration Unit (MMCAU)
- Pseudo Random Number Generator
- Secure Real Time Clock
- DryIce and Tamper Detect
- Cryptographic Acceleration Unit

CONNECTIVITY AND COMMUNICATION

- DSPI
- UART
- I2C

- CAN modules
- USB
- Fast ethernet with IEEE1588
- ISO7816 smartcard interface
- I2S audio interface

USER INTERFACES

- Segment LCD controller
- Graphics LCD controller
- Capacitive touch sensing