FM1 - MPC5XX implementation

This course covers MPC55X and MPC56X NXP MCUs

Objectives

- This training highlights differences between MPC55X and MPC56X.
- The hardware implementation is fully described, especially burst transfers.
- A boot program has been developped.
- The course focusses on PowerPC EABI, which is fundamental for low level programmers.
- A generic interrupt handler supporting nesting is introduced.
- TPU3 functions are studied with the help of a logic analyser.
- QADC operating modes are described.
- The course details the internal debug facilities particularly the MPC56X nexus port.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as QADC and TPU.
• They have been developed with Diab Data compiler and are executed under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related course

- Experience of a 32-bit processor or DSP is mandatory.
- The following course could be of interest:
  - CAN bus, reference IA1 - CAN buscourse

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

MPC5XX OVERVIEW

- MPC5XX block diagram
- Internal resources base address definition
- Pinout and pad types
- PDMCR register programming

THE RCPU

- History buffer
- Propagation of instructions through the pipeline

- Compliance of the RCPU with the programming environment
- Branch unit, static prediction, MPC56X branch target buffer
- Load / store instructions
- Integer arithmetic and logic instructions
- IEEE754 basics
- Float load / store instructions
- Float arithmetic instructions
- The EABI
- Code and data sections, small data areas benefits
- Exception management : handler table, MSR update, automatic interrupt masking
- Requirements to support exception nesting
- Handler table relocation
- Program regions definition and determination of their attributes in the IMPU
- Data regions definition and determination of their attributes in the DMPU

THE USIU MODULE

- Interrupt controller
- IMB peripheral interrupt requests control
- Reset cause enumeration
- Hardware configuration at reset
- Clock synthesizer
- PLL multiplicator selection
- System timers : decrementer, time base, RTC, PIT

HARDWARE IMPLEMENTATION

- Endian modes clarification
- External bus interface, arbitration, read and write timing diagrams
- Dynamic bus sizing
- External decode logic design
- Non wrapping burst transfers
- Memory controller, boot chip select, address decode by means of BRx/ORx registers
- Glueless interface with SRAM and FEPROM

INTERNAL MEMORIES

- CDR3 Flash EPROM, read page buffers, programming and erasing sequences
- Margin reads
- CALRAM: overlay mode operation
- DPTRAM: TPU emulation mode

QADCE MODULES

- Analog inputs multiplexing
- Conversion queue priority scheme
- External trigger
- Programming model
- Result formats

QSMCM MODULES

- UART controller, differences between SC1 and SC2
- Transmit and receive sequences
- SPI protocol explanation
- Command queue
- Transmit and receive sequences

DLCM2 MODULE

- Transceiver interface
- Block and 4x transfers
- J1850 frame format

MIOS14 MODULE

- Counter prescaler submodule
- Counter submodules
- Double action submodules
- PWM submodules
- Real Time clock submodules

TouCAN 2.0B MODULES

- TouCAN organization
- Label filters configuration through the mask registers
- Bit time phases initialization
- Automatique reply

TPU3 MODULES

- Real time hardware events processing
- Channel priority scheme
- Interchannel communication
- QOM and NITC functions introduction
- SPI port emulation

DEBUG FACILITIES

- BDM restrictions : no trace memory
- Watchpoints vs breakpoints
- MPC56X Readi module
- Windriver nexus solution