FM4 - MPC5200 implementation

This course covers the MPC5200 NXP MCU

Objectives

- The course explains how to design a MPC5200 board.
- DDR SDRAM operation is described in order to understand the memory controller programming.
- The 603e core is studied in detail, especially the MMU.
- The course provides examples of internal peripherals software drivers.
- Fast Ethernet controller is viewed in detail.
- The training highlights data paths between PCI and DDR SDRAM.

- This course has been delivered several times to companies developing embedded multimedia equipments.

A lot of programming examples have been developed by ACSYS to explain the boot sequence and the operation of complex peripherals, such as BestComm and Fast Ethernet.
• They have been developed with Diab Data compiler and are executed under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites and related courses

- Experience of a 32-bit processor or DSP is mandatory.
- The following courses could be of interest:
  - Ethernet and switching, reference N1 - Ethernet and switchingcourse
  - PCI, reference IC1 - PCI 3.0course
  - USB Full Speed High Speed and USB On-The-Go, reference IP2 - USB 2.0course

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO MPC5200

Overview

- Innovative IO subsystem
- Dual external bus architecture : SDRAM bus and LocalPlus bus
- Bestcomm features
- Memory map, internal register space

PROCESSOR CORE

603e CORE

- 603e pipeline
- Branch management : static prediction
- Guarded memory
- 603e L1 cache : LRU algorithm, HID0 programming interface
- Software L1 data cache flush
- Cache coherency basics
- JTAG debugger, hardware breakpoint vs software breakpoints
- Branch instructions
- The system call communication path between applications and RTOS
- FPU operation
- The EABI
- Code and data sections, small data areas benefits
- Cache related instructions
- PowerPC timers : TB and DEC
- MMU goals
- The PowerPC address processing
- WIMG attributes definition, page and block access rights definition
- Process protection through VSID selection
- TLB organization, TLB software management
- MMU implementation in real-time sensitive applications
- Exception management
- Requirements to support exception nesting

PLATFORM

SYSTEM INTEGRATION UNIT

- Interrupt Controller routing scheme
- General purpose IO, pin multiplexing
- General purpose Timers
- Slice timers, generation of periodic interrupts
- · Real-Time Clock

HARDWARE IMPLEMENTATION

- Reset configuration
- Clock domains
- Power management
- DDR SDRAM basics
- The DDR SDRAM controller, pinout
- Power-up initialisation, use of the I2C interface
- Initialization of memory controller registers according to a micron DDR SDRAM devices
- External bus interface, modes of operation muxed or non muxed
- Connection to ATA and PCI compliant devices as well as memory-mapped devices
- Chip select programming
- Dynamic bus sizing
- DMA interface
- XLB arbiter, prioritisation, bus grant mechanism

BESTCOMM

- SmartDMA modules, local buffer memory

- Servicing many data streams with individual latency and processing requirements
- Chaining scatter / gather capability
- Task descriptor table
- Function descriptor table

PCI CONTROLLER

- Supported clock ratios
- PCI commands supported as a target and as a master
- XL bus initiator interface
- Endian translation
- XL bus target interface
- Multi-channel DMA transmit interface
- Multi-channel DMA receive interface
- Access to the configuration space
- Programming of inbound and outbound windows
- PCI agent vs PCI host operation mode

INTEGRATED I/Os

USB CONTROLLER

- Data transfer types
- Host Controller interface
- OHCI specification, communication channels
- Root hub partition

CAN CONTROLLER

- The MSCAN controllers, clock system
- Message buffers structure
- ID bit masking
- Arbitration
- Timing and synchronization
- Error management
- Interrupt driven operation

SPI CONTROLLER

- Baud rate selection, transfer delays
- Double-buffered operation
- Transmit and receive sequences

ATA CONTROLLER

- Asynchronous ATA basics, overview of ATA standards
- ATA host controller operation
- Signals and connections
- Sector addressing
- Ultra DMA protocol

FAST ETHERNET CONTROLLER

- MII transfers
- FIFO interface
- Address recognition
- Full and half duplex operation

- Initialization sequence
- MIB block counters

PROGRAMMABLE SERIAL CONTROLLERS

- PSC in UART mode
- PSC in Codec mode
- PSC in AC97 mode
- PSC in Infrared SIR, MIR or FIR mode
- FIFO system

I2C CONTROLLER

- I2C protocol basics
- Transfer timing diagrams, SCL and SDA pins
- Clock synchronization and arbitration
- Transmit and receive sequences