HX2 - Xilinx - Spartan-6 / Virtex-6 Integrated PCI Express Block

This course covers the implementation of the Xilinx PCIe block.

Objectives

- An introduction to PCI Express protocol is done at the beginning to be able later to understand the operation of the back-end bus.
- The course details the parameterizing of the PCI Express core.
- User interfaces are deeply detailed.
- Management of errors and interrupts is studied through examples.
- Guidelines to design the user logic are provided.
- The course targets hard PCI Express cores in the Virtex-6 and Spartan-6 FPGAs.

Xilinx software (ISE) is used to synthesize and implement practical examples, Mentor Graphics ModelSim is used for simulation.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Good knowledge of PCIe gen2 protocol, see our course reference IC4 - PCI Express 3.0course
- Good knowledge of VHDL.
- Experience with simulation tools such as Mentor Graphics ModelSim.
- Basic knowledge of Xilinx ISE software.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

1st DAY

PCI EXPRESS PROTOCOL OVERVIEW

- Introduction to PCI Express
- Transactions types and categories
- Address Space Map and Configuration Space
- PCI type0 basics, PCI express capability structure

PCI EXPRESS AND XILINX CORE GENERATOR

- Selecting link speed and width
- Address decoding logic, BAR registers setting
- TLP buffer sizing
- Power management configuration
- Optional capability structures

SIMULATING A PCIE DESIGN

- Identifying simulation points
- Simulation Methods
- Building TestBench

CONNECTING LOGIC TO THE CORE LOCAL LINK OR AXI INTERFACE

- Clocking and reset
- Common Transaction Interface Signals
- Cut-through vs Store & Forward operation
- Migrating to the integrated block for PCI Express v2.x from v1.x
- AXI interface signals description
- Managing control flow information to optimize the user logic

2nd DAY

DESIGNING A SIMPLE ENDPOINT APPLICATION

- PIO example description
- Endpoint application and PCI Express core connection
- Local Link or AXI interface
- Accessing configuration space from user logic

COMPLIANCE AND DEBUGGING

- Chipscope Pro Description
- Compliance Testing
- Tracking the transitions in the LTSSM (Virtex-6)
- Dynamic reconfiguration (Virtex-6)

ERRORS AND INTERRUPTS

- PCIe Error management, related registers
- Introduction to legacy interrupts, MSI and MSI-X
- Collaborating with PCIe block to generate error messages
- Triggering interrupts, MSI or MSI-X from user logic
- Explaining the benefits of MSI / MSI-X with respect to legacy interrupts