



IC9 - LLI

This course covers the Low Latency Interface (LLI) MIPI bus

Objectives

- *The course starts with an overview of MIPI specification.*
- *The chapters are studied with a bottom-top approach, starting with M-PHY and ending with LLI.*
- *The electrical characteristics and related tests of the M-PHY layer are described.*
- *The course explains the M-PHY state machines and clarifies the configuration of M-PHY through attributes.*
- *LLI bridge from local interconnect to external M-PHY differential pairs is detailed.*
- *All layers of LLI from Physical Adapter to Transaction are explained through Service Access Points and Primitives.*
- *Companies interested in attending this course must adhere to MIPI organization.*
- *This course has been designed for engineers in charge of SoC architecture, functional verification or silicon validation.*

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- *Basic knowledge on digital electronics.*

Course Environment

- *Theoretical course*
 - *PDF course material (in English) supplemented by a printed version for face-to-face courses.*
 - *Online courses are dispensed using the Teams video-conferencing system.*
 - *The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.*
- *At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed*

Target Audience

- *Any embedded systems engineer or technician with the above prerequisites.*

Course Outline

INTRODUCTION TO MIPI SPECIFICATIONS

M-PHY

- *Termination scheme*
- *Signaling schemes*
- *Pulse Width Modulation*
- *M-PHY type I modules*
- *Embedding clock into the bitstream, 8b10b coding*
- *Control symbols*
- *PHY state definition*
- *Transitions between states*
- *HS-MODE BURST Operation*

- *Configuration attributes*
- *Test modes*
- *Electrical characteristics, eye-diagrams*
- *Recommended test functionality*
- *Optical Media Converter*

DEVICE DESCRIPTOR BLOCK (DDB)

- *Services to transfer descriptor and configuration data between devices on a MIPI Interconnect*
- *Underlying interconnect requirements*
- *Accessing DDB Services through DDB Service Access Points*
- *DDB-PDU format*
- *DDB protocol support for Level 1 and Level 2 services*

LOW LATENCY INTERFACE (LLI)

- *Objectives: accessing an external device exactly like a local IP, using memory-mapped transactions*
- *Power management, Automatic Save State*
- *M-PHY Adapter layer*
- *Data link layer, independent flow control using Traffic Classes*
- *Transaction layer, configuration space, ordering rules*
- *Device enumeration*