



IM3 - DSI 1.1

This course covers the Display Serial Interface V1.1 (DSI 1.1)

Objectives

- The course starts with an overview of MIPI specification.
- The layers are described using a bottom-top approach, starting with D-PHY and ending with DSI.
- Forward and Reverse capabilities of a D-PHY are studied.
- The course details the electrical characteristics of D-PHY.
- Access to configuration and status registers through Reverse direction is covered.
- Multi-lane distribution and merging of packets is explained.
- The course focuses on the low level protocol, based on short and long packets used to transport images, embedded data and framing informations.
- Data formats and possible compression of raw data is detailed to understand how the long packet payload is organized.
- Companies interested in attending this course must adhere to MIPI organization.
- This course has been designed for engineers in charge of SoC architecture, functional verification or silicon validation.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge on video transport.

Course Environment

- Theoretical course
 - PDF material in English (printed for face-to-face); online over Teams.
 - Trainer assistance throughout.
- Each session starts with a trainee check-in.

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

Introduction to mipi specifications

D-PHY

- Universal lane module architecture
- Control character usage
- Uni-directional data lanes
- Bi-directional data lanes, turnaround procedure
- Clock lane
- High-Speed data transmission in bursts
- System power states
- Low power states, escape mode
- Low power data transmission

- High-Speed clock transmission
- Fault detection

Display command set (DCS)

- Display architecture
- Power level definition
- Self-diagnostic functions
- Command description
- Pixel-to-byte mapping

Display serial interface (DSI)

- Overview
- Physical layer, flow control
- Multi-Lane Distribution and Merging
- Low-Level Protocol Errors and Contention
- DSI protocol
- DSI conformance test suite
- DSI interoperability test suite