



M4 - 440EPx implementation

This course covers AMCC 440EP and 440EPx processors

Objectives

- The course explains how to design a 440EPx board.
- DDR SDRAM operation is described in order to understand both the electrical interface and the memory controller programming.
- Book E PowerPC architecture is studied through the 440EPx, especially the MMU.
- The training focuses on the new floating point unit.
- The course provides examples of internal peripherals software drivers.
- Gigabit Ethernet controller is viewed in detail.
- The training describes on data flows between PCI bus and internal PLB bus.
- A chapter on Linux porting can be appended on request.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI bus is recommended (see our course reference [IC1 - PCI 3.0course](#)).
- Knowledge of USB is recommended (see our course reference [IP2 - USB 2.0course](#)).

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO 440EPx

- Internal bus organization : dual PLB, OPB, DCR
- Internal concurrent transfers examples
- Hardware implementation : pinout, GPIOs configuration
- 440EPx mapping
- Programming model

CoreConnect PARAMETERIZING

- PLB4-to-PLB3 and PLB3-to-PLB4 bridge parameters

- PLB arbiter, OPB arbiter and PLB4-to-OPB bridge configuration
- Bus errors recovery from syndrome registers
- PLB performance monitor

THE 440 CORE

- Pipeline
- Internal caches
- Speculative loads, storage ordering and synchronization : msync & mbar instructions
- MMU

BOOK E COMPLIANT CORE

- Programming model
- Branch instructions
- Addressing modes, load & store instructions
- Integer instructions
- 16-bit mac instructions to develop DSP algorithms
- Exception management
- Interrupt processing registers
- Core timers
- PowerPC EABI
- JTAG debug
- Real time trace

THE FLOATING POINT UNIT

- IEEE754 basics
- The 440EP FPU features, compatibility with the IEEE754 standard
- Support for single and double precision
- Performance of multiply-accumulate instructions

CLOCKS, RESET AND POWER MANAGEMENT

- Clocks synthesizer
- PCI clocking
- Low power modes
- Reset signals
- Initialization software requirements
- IIC bootstrap controller

INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS

- Interrupt source enumeration
- Interrupt masking and acknowledgement explanation
- Critical interrupt handlers using vectorization
- General Purpose Timers

THE DDR-SDRAM CONTROLLER

- DDR-SDRAM operation : a 128-Mbits DDR-SDRAM from Micron is used as an example
- Command truth table
- Hardware interface, SSTL-2 termination logic
- Bank activation, read, write and precharge chronograms
- ECC error correction
- Introduction to 440EP DDR-SDRAM controller
- Address decode
- Timing parameters programming

- Initialization routine

THE EXTERNAL BUS CONTROLLER

- The bridge between external bus and PLB, read and write buffers
- Dynamic bus sizing
- Address decoding in bank registers to control the chip-select signals
- Timing parameters initialization
- Device-paced transfers
- External bus master interface
- The NAND Flash controller
- Direct interfacing to discrete NAND flash devices (up to 4 devices), SmartMedia card socket

THE PCI BRIDGE

- Explaining the data path within the bridge for read and write transactions
- Configuration cycles
- Setting translations between local memory space and PCI MEM space (outbound transactions), and between PCI MEM space and local memory space (inbound transactions)
- Error handling
- Arbitration algorithm

THE 4 DMA CHANNELS

- Overview of the DMA to PLB4 and DMA to PLB3 controllers
- The buffered transfer mode
- Related signals
- Channels bus priority
- Data packing / unpacking
- Buffers chaining

THE GIGABIT ETHERNET CONTROLLER

- 802.3 specification fundamentals
- 440EPx Ethernet controller organization : EMAC and MAL modules, reasons of their independence
- Possible PHY interfaces
- The addressing modes : unicast, multicast, broadcast and promiscuous
- Hash table interest for switch applications
- Buffer descriptors mechanism, wrapping
- Transmit sequence
- Receive sequence
- Buffer descriptors initialization
- Interrupt management

THE SECURITY MODULE

- Introduction to encryption
- On-chip Ipsec / SSL Security acceleration engine
- Public key acceleration

THE USB INTERFACES

- USB protocol fundamentals
- Internal vs external transceiver
- USB2.0 device interface
- USB1.1 host interface
- Dedicated DMA
- UTMI bus

THE UARTS

- UART description
- The UART frame : break, idle, start, stop
- Transmission and reception FIFOs use
- Flow control signals management

THE SPI PORT

- SPI protocol fundamentals
- Clock polarity and phase selection
- Transmit and receive sequences

THE IIC PORTS

- IIC protocol fundamentals
- Transfer chronograms, IIC_SCL and IIC_SDA pins
- Transmission and reception sequence