



## M6 - 440GR/GRx implementation

*This course covers AMCC 440GR and 440GRx processors*

### Objectives

- The course explains how to design a 440GRx board.
- DDR SDRAM operation is described in order to understand both the electrical interface and the memory controller programming.
- Book E PowerPC architecture is studied through the 440GRx, especially the MMU.
- The course provides examples of internal peripherals software drivers.
- Gigabit Ethernet controller is viewed in detail.
- The training explains how to optimize the internal data paths that exist between PowerPC core, memory and PCI interfaces.
- A chapter on Linux porting can be appended on request.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.

A more detailed course description is available on request at [training@ac6-training.com](mailto:training@ac6-training.com)

### Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI bus is recommended (see our course reference [IC1 - PCI 3.0course](#)).
- Knowledge of Gigabit Ethernet is recommended, see our course reference [N1 - Ethernet and switchingcourse](#).

### Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

### Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

## Course Outline

### INTRODUCTION TO 440GRx

- Internal bus organization : dual PLB, OPB, DCR
- Internal concurrent transfers examples
- Hardware implementation : pinout, GPIOs configuration
- Internal SRAM
- Programming model

### CORECONNECT PROGRAMMING INTERFACE

- PLB, OPB and DCR bus features

- PLB4-to-PLB3 and PLB3-to-PLB4 bridge parameters
- PLB arbiter, OPB arbiter and PLB4-to-OPB bridge configuration
- PLB performance monitor

## **440 CORE**

- Pipeline
- Internal caches
- Speculative loads
- MMU

## **BOOK E COMPLIANT CORE**

- Programming model
- Branch instructions
- Addressing modes
- Integer instructions
- 16-bit mac instructions
- Exception management
- Interrupt processing registers
- Exception priorities
- Core timers
- PowerPC EABI
- JTAG debug
- Real time trace

## **CLOCKS, RESET AND POWER MANAGEMENT**

- Clocking
- Low power modes
- Reset signals
- Initialization software requirements
- IIC bootstrap controller

## **INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS**

- Interrupt source enumeration
- Interrupt masking and acknowledgement explanation
- Critical interrupt handlers using vectorization
- Interrupts priority
- General Purpose Timers modes of operation

## **THE DDR2-SDRAM CONTROLLER**

- DDR-SDRAM operation
- Jedec specification basics
- Differences between DDR1 and DDR2 SDRAMs
- Command truth table
- Refresh types
- Bank activation, read, write and precharge timing diagrams
- ECC error correction
- Introduction to the 440GRx DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Address decode
- Timing parameters programming
- Initialization routine

## THE EXTERNAL BUS CONTROLLER

- External bus pinout
- Dynamic bus sizing
- Address decoding
- Boot ROM size definition
- External bus master interface
- The NAND Flash controller
- Direct interfacing to discrete NAND flash devices

## THE PCI BRIDGE

- Inbound transactions handling, Outbound transactions handling
- Configuration cycles
- Setting translations between local memory space and PCI MEM space (outbound transactions), and between PCI MEM space and local memory space (inbound transactions)
- Error handling

## THE 4 DMA CHANNELS

- Overview of the DMA to PLB4 and DMA to PLB3 controllers
- The buffered transfer mode
- Burst mode support
- Channels bus priority
- Data packing / unpacking
- Buffers chaining

## THE GIGABIT ETHERNET CONTROLLER

- 802.3 specification fundamentals : the 3 layers PHY, MAC and control
- Frame format with and without VLAN option
- 440GRx Ethernet controller organization
- PHY interface : GMII, MII, RGMII, TBI, RTBI, SMII
- Frame filtering
- Buffer descriptors mechanism, wrapping
- Buffer descriptors initialization
- Interrupt management
- Errors management

## THE UARTS

- UART description
- The UART frame : break, idle, start, stop
- Transmission and reception FIFOs use
- Flow control signals management

## THE SPI PORT

- SPI protocol fundamentals
- Clock polarity and phase selection
- Transmit and receive sequences

## THE IIC PORTS

- IIC protocol fundamentals : addressing, multimaster operation
- Transmission and reception sequence
- Bit rate programming