M8 - 460SX / 460GTx implementation

This course covers AMCC 460SX and 460GTx Power processors

Objectives

- The course explains how to design a 440GTX board.
- DDR2 SDRAM operation is described in order to understand both the electrical interface and the memory controller initialization.
- Note that this course contains only an overview of the IBM Microelectronics PPC464 PowerPC core.
- The architecture of the 440GTX, based on CoreConnect, is explained in order to understand how to tune the performance of the internal crossbar.
- The Gigabit Ethernet controller is viewed in detail.
- The training explains how to optimize the data paths that interconnect PPC core, PCIe bridge and memory interface.
- The course also details the operation of the cryptographic engine.

Labs are compiled with Diab Data compiler and run under Lauterbach debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.
- Knowledge of PCI Express is recommended, see our course reference IC4 - PCI Express 3.0course .

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO 460GTX

SOC ARCHITECTURE

- Internal bus organization: dual PLB, OPB, DCR
- 2-way 12 master crossbar
- Internal concurrent transfers examples
- Hardware implementation: pinout, GPIOs configuration
- 440GTX mapping
- Programming model

CORECONNECT

- Primary PLB segment, Low Latency slaves and High Bandwidth slaves
- Secondary PLB segment
- PLB Master and Slave Assignments
- Bus errors recovery from syndrome registers
- Target Directed Completion

PPC464 CORE

THE CORE ARCHITECTURE

- 7-stage pipeline operation
- Speculative execution, guarded memory
- Serialization
- Cache basics
- Data flow between external memory and caches
- Process vs thread
- Memory Management Unit
- Translation Lookaside Buffer initialization
- Speculative loads, msync and mbar instructions

BOOK E COMPLIANT CORE

- Branch instructions
- Addressing modes, load & store instructions
- Integer instructions
- 16-bit mac instructions to develop DSP algorithms
- Exception management
- Core timers
- PowerPC EABI
- Real time trace

THE FLOATING POINT UNIT

- IEEE754 basics, floating points numbers encoding
- The 440GTX FPU features, compatibility with the IEEE754 standard
- Support for single and double precision
- Floating point load / store instructions
- Performance of multiply-accumulate instructions
- Management of denormalized numbers
- FPU exceptions

ON-CHIP SRAM / L2 CACHE

- Write-through look-aside cache
- Understanding the data / instruction path between memory, L2 cache and L1 instruction and data caches
- Hardware cache coherency
- Configuration as SRAM to accelerate the processing of incoming Ethernet packets
- Dedicated on-chip SRAM

SOC PLATFORM

CLOCKS, RESET AND POWER MANAGEMENT

- Clocks synthesizer, PLL multiplicators definition during SysReset, IIC bootstrap controller clocking
- PCIe clocking
- Low power modes
- Reset signals, reset types, processor state according to the reset type

- Initialization software requirements
- IIC bootstrap controller

INTERRUPT CONTROLLER & GENERAL PURPOSE TIMERS

- Interrupt source enumeration
- Interrupt masking and acknowledgement explanation, UICx_ER and UICx_SR registers
- Critical interrupt handlers using vectorization
- Interrupts priority
- General Purpose Timers

THE DDR-SDRAM CONTROLLER

- Memory subsystem, Memory Queue Module (MQ)
- Three parallel paths from PLB to memory
- DDR2-SDRAM operation
- Differences between DDR1 and DDR2, On-Die Terminations
- Jedec specification
- Hardware interface, SSTL-2 termination logic
- Bank activation, read, write and precharge timing diagrams
- ECC error correction
- Introduction to the 440GTX DDR-SDRAM controller
- Initial configuration following Power-on-Reset
- Look-ahead request queue
- Page mode
- Initialization routine

THE EXTERNAL BUS CONTROLLER

- The bridge between external bus and PLB
- Address decoding in bank registers to control the chip-select signals
- Timing parameters initialization for either bursting or non bursting devices
- Boot ROM size definition
- Device-paced transfers
- Special cycle, error reporting
- The NAND Flash controller
- Boot from NAND

THE PCI EXPRESS BRIDGES

- Bridge features, 8-lane or two 4-lane port
- Configuration as Root Complex or EndPoint
- Inbound transactions handling, Outbound transactions handling
- Setting translations between local memory space and PCI MEM space
- Interrupt management (legacy INT, MSI, MSI-X)
- Advanced error reporting
- Boot modes, initialization / Reset sequence
- Synchronizing CPUs through I2O controller, messages and doorbells

THE 4 DMA CHANNELS

- The buffered transfer mode
- Burst mode support
- Related signals, *DMMAck signal timing programming
- Channels bus priority
- Data packing / unpacking
- Buffers chaining through the scatter / gather mode, descriptors table initialization

THE SECURITY MODULE

- Introduction to encryption
- On-chip Ipsec / SSL Security acceleration engine
- Encryption DES, 3-DES, AES, ARC-4
- Storage encryption engine

ENHANCED DMA CONTROLLER

- Description of the 3 channels
- RAID acceleration on DMA channels 0 and 1 (460SX only)
- Encryption support on DMA 0
- Command descriptor block structure

INPUTS / OUTPUTS

THE GIGABIT ETHERNET CONTROLLERS

- 802.3 specification fundamentals: the 3 layers PHY, MAC and control
- Frame format with and without VLAN option
- 440GTX Ethernet controller organization: EMAC and MAL modules, reasons of their independence
- PHY interface: GMII, RGMII interfaces
- Frame filtering: unicast, multicast, broadcast and promiscuous
- Hash table utilization in switch applications
- Buffer descriptors mechanism, wrapping
- Errors management
- Two ports support TCP/IP acceleration, checksum processing
- Interrupt coalesces support
- IEEE1588 timestamp and clock synchronization support

THE UARTS

- NS16570-likeUART description
- Transmission and reception FIFOs usage
- Flow control signals management
- Moving transmit / received data with DMA

THE IIC PORTS

- IIC protocol fundamentals: addressing, multimaster operation
- Transmission and reception sequence
- Port 0 supports serial Bootstrap ROM with default override parameters at initialization