



NS1 - MARVELL 88E6061/6061B/6031 Ethernet switches

This course covers Marvell Link Street 100 Mbps Soho switches

Objectives

- Providing the basic knowledge on 802.3 and 802.1.
- Understanding the parameters that determine the QoS.
- Implementing the Dynamic Queue Limit architecture.
- Description of the Address Lookup engine.
- Clarifying the bridge loop prevention mechanism.
- Becoming familiar with the API defined by Marvell.
- This course has been delivered several times to companies involved in the design of embedded equipments.

Practical labs using the Marvell GUI allow attendees to understand the various operation modes offered by this class of switch devices.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Knowledge of IEEE 802.3 and IEEE 802.1: see our course Ethernet and switching, reference [N1 - Ethernet and switching](#) course

Course Environment

- Theoretical course
 - PDF course material (in English) supplemented by a printed version for face-to-face courses.
 - Online courses are dispensed using the Teams video-conferencing system.
 - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

100 Mbps ETHERNET BASICS

- MAC layer
- PHY layer
- Auto-negotiation

802.1Q BASICS

- Spanning tree
- VLAN tag
- Management functions
- Automatic address learning
- Handling multicasts, GVRP

INTRODUCTION TO 88E6061 SWITCHES

- Block diagram
- Application examples
- Software architecture

SWITCH CORE FUNCTIONAL DESCRIPTION

- Architecture, embedded memory
- Operation of the integrated MACs
- IGMP snooping
- Ingress policy
- Queue controller
- Egress policy
- Spanning tree support
- Handling of management frames

PHY INTERFACE

- Transmit PCS and PMA
- Receive PCS and PMA
- Far End Fault indication
- Auto MDI/MDIX crossover
- Accessing PHY registers, MDC/MDIO interface
- Register description
- Auto-configuration

SOFTWARE ARCHITECTURE

- Multi-layer architecture
- Source code organization
- Platform specific routines
- SMI interface functions
- Semaphore related routines
- Accessing global registers
- API layer