P4 - CoreConnect

This course covers the CoreConnect specification, explaining PLB, OPB, DCR buses and bridges

Objectives

- The course describes the 3 buses specified by the IBM CoreConnect specification : PLB, OPB and DCR.
- It explains also the operation of bus bridges PLB-to-OPB and OPB-to-PLB.
- All parameters of the Xilinx CoreConnect infrastructure logicores are described in detail.
- Labs have been developed to become familiar with the simulation toolkit : Bus Functional Models (BFM) and CTG (CoreConnect Test Generator).
- The course focuses on bus error recovery through syndrome registers.
- 128-bit PLB, also known as PLB4, is fully covered including 2-way crossbar implementation.
- The course explains how to tune programmable parameters through the PLB performance monitor.

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- This training has been delivered several times to engineers developing ASICs based on Power cores and to engineers developing SoCs based on Xilinx FPGAs containing Power cores.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a parallel digital bus is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO CoreConnect

- SoC organization
- Intellectual Property reuse by using common bus for inter-macro communication
- The IBM 3-bus for interconnecting cores : PLB, OPB and DCR
- Benefits of DCR compared to memory-mapped IOs
- The infrastructure cores developped by Xilinx

THE PLB

- · Arbitration

- · Bus time-out detection
- · Locked transfer
- · Address pipelining capability
- · Differences between a 1-deep and a N-deep (N>2) pipeline implementation
- Single data, burst and line transfer timing diagrams
- Read burst and write burst terminations
- Dynamic bus width adaptation
- PLB usage in Xilinx FPGAs
- The PLB Xilinx logicore

FIXING BUS ERRORS

- Parity generation and checking
- Slave error report to masters
- Syndrome registers

THE PLB PERFORMANCE MONITOR

- Use of the PPM to tune programmable parameters
- Event counting, duration measurement
- Connection of the PPM to the PLB fabric
- Pipeline stage usage tracking

PLB ARBITRATION

- Central arbitration mechanism
- Fixed and rotative priority schemes
- PLB watchdog timer
- Programming interface
- Xilinx PLB arbiter operating modes

THE 128-BIT 2-WAY CROSSBAR

- Concurrent read transactions and concurrent write transactions
- Highlighting address path, read data path and write data path
- Selecting the slave bus segment, PCBC register programming

THE OPB

- · Dynamic bus sizing vs Byte Enables
- · Distributed multiplexing
- Arbitration
- OPB interface for master, slave, arbiter and DMAs
- Slave retry
- Logicore Xilinx OPB with OPB arbiter
- Connection to OPB through IPIF

THE PLB-to-OPB BRIDGE

- Block diagram and data flows
- Internal data buffers structure
- PLB-to-OPB signals
- Bridge control registers
- Xilinx PLB-to-OPB bridge user configurable parameters
- Definition of address ranges allowing PLB masters to access the OPB bus

THE OPB-to-PLB BRIDGE

- Block diagram and data flows
- Internal data buffers structure
- Synchronization with the PLB-to-OPB bridge
- Bridge control registers
- Xilinx OPB-to-PLB bridge user configurable parameters
- Definition of address ranges allowing OPB masters to access the PLB bus

THE DCR BUS

- Features
- Bus operation : bypass mux use
- The DCR Xilinx logicore

SIMULATING CoreConnect BUSES

- Description of the simulation tools provided by IBM Microelectronics : BFMs and CTG
- Step-by-step explanation of the simulation flow
- Development of a testbench to test a PLB IP