P5 - PPC476 core implementation

This course covers the PowerPC 476FP core, including L2 cache and PLB6 interface

Objectives

- A boot firmware that initializes the MMU has been developped.
- Internal debug facilities are described.
- The course focuses on PPC476 low level programming, especially the PowerPC EABI.
- Examples of exception handlers are provided.
- The course also covers the debug architecture.
- A FFT has been developed to explain how to use MAC instructions.
- The Floating Point Unit operation is described.
- Note that this course also includes the PLB6 interconnect.

Labs are compiled with GNU compiler and run under Lauterbach Trace32 debugger.
A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Course Outline

INTRODUCTION TO PPC476FP

- Internal architecture overview
- Connection to peripheral IPs
- Clocking
- Programming model, the 4 register groups GPRs, SPRs, DCRs and memory mapped

INSTRUCTION PIPELINE

- 5-stage pipeline operation, 4-issue architecture
- Branch Target Address Cache
- Speculative execution, guarded memory
- Register renaming
- Serialization

EXCEPTION MECHANISM AND TIMERS

- Exception processing
- Critical versus non critical interrupts
- Syndrome registers updating according to the exception source
- Building the vector table
- Core timers: PIT, FIT and WDT
- Reset configuration

MEMORY MANAGEMENT UNIT

- Introduction to MMU, Process vs thread
- Unified Translation Lookaside Buffer organization
- Level 1 separate instruction and data TLBs, level 2 unified TLB
- Address translation
- Clarifying the purpose of the hash function
- Describing the Tag array
- Bolted entries
- MMU related exceptions
- UTLB coherency

L1 CACHES

- Cache basics
- 4-way set associative organization, LRU replacement algorithm
- Cache programming interface
- Cache related instructions
- Double line fetch enable
- Locking capability
- Cache control and debugging features
- Instruction cache synonyms

L2 CACHE

- Four-way set-associative level 2 cache design
- Modified/exclusive/shared/invalid, tagged, shared last, modified unsolicited (MESI+T+SL+MU) protocol coherencu
- Cache operation instructions
- Understanding how data / instructions are transferred from memory to L1 and L2 caches
- Preloading the L2 cache
- Reservation management
- L2 cache performance monitor
- CPU L1 Cache Interface Registers

DATA PATH

- Clarifying the steps required to load a data cache line, utilization of refill buffers
- Use cases for lwsync, msync, mbar and eieio instructions
- Self-modifying code sequence
- Store gathering support

POWER INSTRUCTION SET ARCHITECTURE V2.05 COMPLIANT CORE

- Branch instructions, restrictions regarding regions that can be accessed by direct branches
- System call instruction: link between applications and RTOS
- Addressing modes
- Byte reverse instructions to access PCI/PCIe configuration space
- Semaphore management with lwarx / stwcx. instructions

- Arithmetical and logical instructions, shift and rotate instructions
- The PowerPC EABI
- Self-modifying code sequence
- 16-bit mac instructions to develop fixed point DSP algorithms

FLOATING POINT UNIT

- IEEE754 basics
- Six-stage super-pipelined floating-point arithmetic execution
- Floating point exceptions
- Data handling and precision

INTEGRATED DEBUG FACILITIES

- Invasive debug with JTAG
- Non invasive debug with trace port
- Hardware vs software breakpoints
- Range Inclusive / Exclusive Comparison Mode
- Data value comparison
- Debug related interrupts

HARDWARE IMPLEMENTATION OF THE PPC476FP CORE

- Clock and power management interface
- CPU control interface
- Reset interface
- External interrupt controller interface
- Instruction-side local bus interface
- Data-side local bus interface
- DCR interface

PLB6

- Separate interfaces for masters, slaves and snoopers
- Supports SMP coherency, with 7 cache states
- Coherency State Transition Tables
- Coherent data intervention
- Command definitions, clarifying what is a RWITM, a RWNITC
- Transfer protocol, address phase
- Master Retry Requirements
- Hang Detect and Resolution Requirements
- Snoop Partial Response Requirements
- Ordering Requirements